THE HONORABLE JAMES L. ROBART

UNITED STATES DISTRICT COURT
WESTERN DISTRICT OF WASHINGTON
AT SEATTLE

MICROSOFT CORPORATION, a Washington corporation, Plaintiff, v. MOTOROLA, INC., and MOTOROLA MOBILITY, INC., Defendants. MOTOROLA MOBILITY, INC., and GENERAL INSTRUMENT CORPORATION, Plaintiffs/Counterclaim Defendant, v. MICROSOFT CORPORATION, Defendant/Counterclaim Plaintiff.	Case No. C10-1823-JLR DECLARATION OF TIMOTHY J. DRABIK IN SUPPORT OF MOTOROLA, INC. AND MOTOROLA MOBILITY, INC.'S RESPONSE TO MICROSOFT CORPORATION'S MOTION FOR SUMMARY JUDGMENT OF INVALIDITY **NOTED: Friday, April 13, 2012** **ORAL ARGUMENT REQUESTED**

I, TIMOTHY J. DRABIK, hereby declare as follows:

I make this Declaration on personal knowledge, unless specifically stated otherwise.

I. INTRODUCTION

A. Background

1. I received Bachelor of Science degrees in Electrical Engineering and in Mathematics from the Rose-Hulman Institute of Technology in 1981, and Master of Science and Ph.D. degrees

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in Electrical Engineering from the Georgia Institute of Technology in 1982 and 1990, respectively.

2. Through my formal education, I acquired a background in mathematics, applied physics, system theory and signal processing, optics and optical engineering, microelectronics fabrication, and integrated circuit design. This background facilitated my academic and industrial research and development activities. I have 30 years of collective experience in signal and image processing, high-performance computing, analog and digital integrated circuit design, optics and optical engineering, liquid crystal displays, microelectronics and integrated circuits, optoelectronics, device fabrication and packaging, and optical telecommunications. I have worked in industry and done academic research. I also have coded extensively in various software languages, including FORTRAN, C, and Matlab, and I used Verilog in the design process for a graduate course in IC design.

B. <u>Preparation</u>

3. I am an expert in the field of signal processing, and I have been retained by Motorola as a consultant and expert witness in this action.

4. I have read and studied United States Patent Nos. 7,310,374 (the "'374 patent"), 7,310,375 (the "'375 patent"), and 7,310,376 (the "'376 patent") (collectively, the "Motorola Patents").[1] I have also reviewed the file histories of the Motorola Patents.

5. Based on my review of these materials and my prior experience in the field of signal processing, I have developed a technical understanding of the subject matter of the Motorola Patents.

6. I am informed that questions have arisen about the structure described in the '374, '375 and '376 patents for performing functions contained in certain elements of '374 patent, claim 14, '375 patent, claim 13, and '376 patent, claim 22. I submit this declaration to explain how, in

[1] Copies attached as Exhibits A, B, and C. The Motorola Patents have a common specification. For ease of reference, I will use the '374 patent for my citations.

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my opinion, a person of ordinary skill in the art of video coding would understand the structure identified in the Motorola Patents for performing these claimed functions.

II. LEVEL OF ORDINARY SKILL IN THE ART

7. In my opinion, the art pertinent to the subject matter of the Motorola Patents is the art of video coding, which is a subset of signal processing that focuses on digital video signals.

8. A person of ordinary skill in the art as of 2001-2002 would have at least a Bachelor's degree in electrical or computer engineering or equivalent and at least three years of experience working in the field, or would have a Master's degree in electrical or computer engineering or equivalent and at least one year of experience working in the field.

9. In 2001/2002, I had over 20 years of academic and industry experience with technologies, systems, and signal processing for information processing and display. In particular, as I mentioned earlier, I had taught courses in applied mathematics, digital signal processing, Fourier optics and holography, optical information processing, information theory, pattern recognition, semiconductor electronics, integrated circuit design, and linear system theory to undergraduate and graduate students. Also, at AT&T Bell Labs during the early 1980s, I designed hardware for fiber-to-the-home systems and investigated options for video bandwidth compression and coding. With Displaytech in 2001 and 2002, I addressed problems that arise in the display of moving color images and clocking problems that become more difficult as display resolution increases.

III. OVERVIEW OF THE PATENTS

10. The claims at issue in Microsoft's motion are all directed to "[a]n apparatus for decoding an encoded picture from a bitstream." '374 patent, claim 14, '375 patent claim 13, and '376 patent, claim 22. The bitstream is a stream of data representing digital video content comprising a stream of pictures. '374 patent, 1:33-34. In the bitstream, the digital video content

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is represented in compressed, or encoded, form. *Id.* at 1:59-67. Decoding the encoded pictures involves processing the bitstream to decompress the video data. *Id.*

11. Numerous video coding methods have been developed. *Id.* at 2:9-19. To successfully decode an encoded picture, a decoder must recognize the format in which an encoder has rendered the video data. *Id.* Therefore, video coding standards have been developed to standardize the various video coding methods. *Id.*

12. Uncoded digital video content includes redundant data. For example, a picture in a stream of pictures may have an area that has the same or similar brightness and/or color as another area of a previous picture in the stream, or another area of the same picture. Compression takes advantage of these temporal (picture to picture) and spatial (within the same picture) redundancies by removing data that is "non-essential," to decrease the amount of data that must be transmitted in the bitstream. *Id.* at 1:59-62, 2:1-5. Decoding replaces the data that was removed. *Id.* at 1:62-67. Most modern video coding standards, such as those developed by MPEG and ITU, are based on an algorithm for removing temporally redundant data called "temporal prediction with motion compensation." *Id.* at 2:20-25. One aspect of this algorithm involves predicting video data representing an area of a picture from video data representing an area or areas of one or two other pictures called reference pictures. *Id.* at 2:26-41. This is called "inter coding." *Id.* at 9:9-14. Prediction of an area of a picture can also be based solely on other areas within the same picture. Prediction within a single picture is called "intra coding." *Id.* at 9:11-13.

13. The Motorola Patents refer to prediction and predicted pictures in the Abstract, Background (*Id.* at 2:20-41), the Summary of the Invention (*Id.* at 2:54-56), and throughout large portions of the Detailed Description (*Id.* at 5:4-53, 5:65-67, 6:1-37, 7:1-3, 7:50-53, 7:65-67, 8:33-36, 8:42-43, 9:15-12:56 (describing inter prediction), 14:37-16:63 (describing intra prediction). Included in these descriptions are methods and rules to be followed when encoding and decoding predicted pictures in which adaptive frame/field (AFF) coding is used. The Motorola Patents further describe that the blocks within each macroblock pair in frame mode or field mode can be

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intra coded or inter coded. *See, e.g., Id.* at 9:46-59 (the blocks "can be in either frame or field mode"), 10:34-37 (referring to "macroblock pair based AFF" in context of inter coding), 11:28-31 ("[t]his method [inter coding method] can be used in ... pair based macroblock AFF coding"), 14:64-65 ("An intra block and its neighboring blocks may be coded in frame or field mode."), 15:48-49 ("Block C and its neighboring blocks A and B can be in frame mode or field mode."), 15:64-65 ("In the case of decoding the prediction modes of blocks ..."), 16:12-23, **(**"If the above macroblock pair (170) is decoded in field mode ..."), 16:24-35 **(**"if the above macroblock pair (170) is decoded in frame mode ...").

14. The problem that Motorola's macroblock pair AFF coding invention solved related to prediction. A basic problem with prediction techniques prior to the invention was that a macroblock coded in field mode could not be divided the same seven ways as a macroblock in frame mode. For single macroblock based AFF, a field macroblock was first divided into a 16×8 pixel top field and a 16×8 pixel bottom field. *Id.* at 7:4-14. The field macroblock could be divided *only* five different ways. *Id.* at 7:15-24. The block sizes of 16×16 pixels and 8×16 pixels were not available for a macroblock encoded in field mode because, in field mode, a block could not contain lines from both the top and bottom fields. *Id.* at 7:27-33. This is called the single parity requirement. *Id.* Because all seven block sizes were not available in field mode, prediction performance suffered. The Motorola Patents describe the problem with prior prediction techniques as follows:

> This implies that the performance of single macroblock based AFF may not be good for some sequences or applications that strongly favor field mode coding. *Id.* at 7:33-36.

15. The solution arrived at by the Motorola inventors was to use multiple neighboring macroblocks instead of a single macroblock for AFF coding. For example, FIG. 7 shows a vertical pair of macroblocks that can be used in AFF coding. The Motorola Patents describe the solution as follows:

> In order to guarantee the performance of field mode macroblock coding, it is preferable in some applications for macroblocks that are coded in field mode to have the same block

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> sizes as macroblocks that are coded in frame mode. This can be achieved by performing AFF coding on macroblock pairs instead of on single macroblocks." *Id.* at 7:37-43.

16. With Motorola's invention of AFF coding on macroblock pairs, the macroblocks of a frame based macroblock pair "can be further divided into the smaller blocks of FIGS. 3a-f for use in the temporal prediction with motion compensation algorithm." *Id.* at 7:50-53. And, because the top field macroblock and the bottom field macroblock of a field based macroblock pair are both 16×16, each field macroblock "can now be divided into one of the possible block sizes of FIGS. 3a-f" (*i.e.*, the same seven ways as a 16×16 frame macroblock). *Id.* at 7:65-67. This provided greater flexibility for use in prediction, which led to more efficient video encoders and decoders.

IV. THE PATENTS TEACH TO USE THE WELL-KNOWN STRUCTURE OF A DECODER TO PERFORM THE CLAIMED FUNCTIONS

17. A person of ordinary skill in the art, reading the common specification of the Motorola Patents, would understand these patents to teach using a decoder to perform the functions in claim 14 of the '374 patent, claim 13 of the '375 patent, and claim 22 of the '376 patent.

18. Each claim refers to "an apparatus for decoding an encoded picture from a bitstream." As I discuss further below, this would be understood by a person of ordinary skill in the art as a description of the purpose of a well-known class of structures called digital video decoders.

19. Digital video decoders are a class of electronic devices that decode, or decompress, encoded digital video content. The specification describes the general idea behind decoding:

> After the compressed video data has been transmitted, it must be decoded, or decompressed. In this process, the transmitted video data is processed to generate approximation data that is substituted into the video data to replace the "non-essential" data that was removed in the coding process. '374 patent at col. 1:62-67.

20. A person of ordinary skill in the art would understand that digital video decoders have well-known, basic structural components for decoding encoded digital video content – entropy

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decoding, inverse scanning, inverse quantization, inverse transform and prediction. These components invert the processes used to encode the video data: entropy decoding is the inverse of equally well-known entropy coding, inverse scanning is the inverse of equally well-known scanning, inverse quantization is the inverse of equally well-known quantization, inverse transform is the inverse of equally well-known transform, and inverse prediction is the inverse of equally well-known prediction.

21. A person of ordinary skill in the art would further understand that these components are typically configured to recognize digital video content encoded in one or more standardized encoding formats, in accordance with industry standards. The specification identifies MPEG-1, MPEG-2, MPEG-4, H261 and H263 as examples of video coding standards in wide use. '374 patent, 2:9-19.

22. The specification further informs the person of ordinary skill that the invention is compatible with a digital video decoder configured to decode digital video content encoded in accordance with the MPEG-4 Part 10 AVC/H.264 standard. *Id.* at 1:17-20, 4:35-51.

23. These uses of "decoder" in the specification, in combination with the reference to well-known MPEG/ITU-T video coding standards, connote to a person of ordinary skill in the art that the "decoder" referred to in the specification is a discrete, well-known class of structures called digital video decoders, which have the basic functional blocks discussed above.

24. At the time of the filing of the specification, the known class of digital video decoders included several types of electronic devices, including devices that used different technologies to implement components of the decoder. Accordingly, the specification describes that a decoder can be implemented in the following ways:

> The encoder or decoder can be a processor, application specific integrated circuit (ASIC), field programmable gate array (FPGA), coder/decoder (CODEC), digital signal processor (DSP), or some other electronic device that is capable of encoding the stream of pictures. ... The term "decoder" will be used to refer expansively to all electronic devices that decode digital video content comprising a stream of pictures. '374 patent, 4:59-5:3.

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25. In the art of digital systems design, so called "hardware description languages," such as Verilog, are used to describe a system to be implemented. A person of ordinary skill in the art would have understood how to write Verilog code for the well-known decoder and that, for example, a single Verilog description of a decoder could be effectively "cast" into different target technologies, such as ASIC, FPGA, DSP, etc. This concept of implementation flexibility is routinely taught to undergraduates in the field.

26. A person of ordinary skill in the art would have understood that any of the electronic devices in the class of digital video decoders would have analogous implementations of the basic structural components that I discussed above. In an ASIC implementation, the various structural components correspond directly to hard-wired physical blocks of circuitry. In an FPGA implementation the structural components are configured through programming of connections among circuit elements. Once programmed, an FPGA possesses physical blocks of circuitry corresponding to functional blocks, just as an ASIC does. With respect to software implementations on a processor or a DSP, the various structural components are defined by procedures or software tasks, through which video data is processed.

27. Implementations of digital video decoders of each of the types described in the specification were known.

28. An illustration of a known ASIC structure for a decoder can be found, for example, in the datasheet for the Sigma Designs EM847x family of single-chip MPEG audio/video decoders (Copy attached as Exhibit D to this Declaration). This datasheet is dated March 18, 2002. A person of ordinary skill in the art would have appreciated that such decoders were commercially available at that time. As shown on p. 3 of the datasheet, decoders known at that time included the basic structural building blocks of entropy decoding (*i.e.*, MPEG-1&2 Huffman; MPEG-4 Huffman), inverse scanning (*i.e.*, ZigZag), inverse quantization (*i.e.*, Inverse Quantization), inverse transform (*i.e.*, IDCT), and inverse prediction (*i.e.*, AC/DC Predictor; Motion Compensation):

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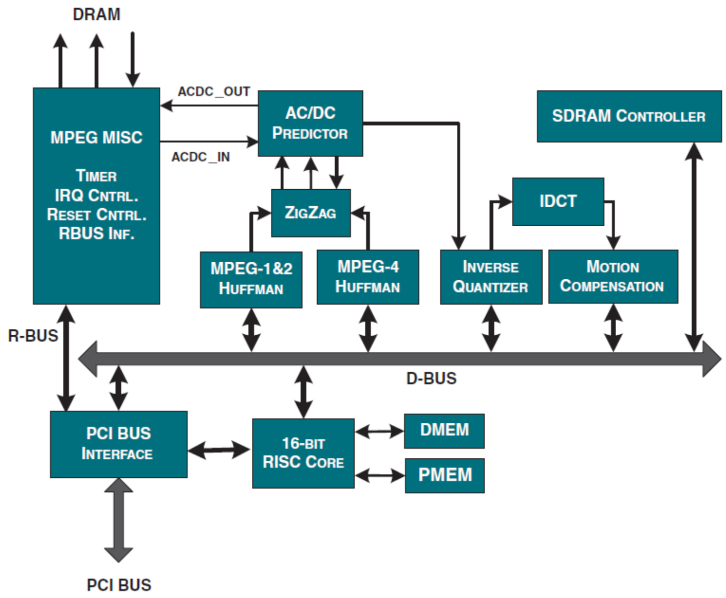

29. An illustration of how these various building blocks were known to those of ordinary skill in the art can be found, for example, in the explanation of each block on pp. 3-4, where these blocks are described without further elaboration:

MPEG-1 and MPEG-2 Huffman Decoder

The MPEG Video Decoder engine uses the Huffman Decoder as its front end. It can decode either a MPEG-1 or MPEG-2 formatted data stream. The Huffman Decoder is commanded directly from the RISC processor. It extracts fixed-length, variable-length or start codes from the bitstream and returns the value to the RISC processor or passes it directly to the Inverse Quantizer. The Huffman Decoder can also do tasks such as decode the macroblock increment address, get the macroblock type, get coded block pattern, get motion vector codes and decode a delta motion vector.

MPEG-4 Huffman Decoder

The MPEG-4 Huffman Decoder is the front-end to the MPEG-4 engine. It provides specialized instructions to the RISC processor to enable the decoding of Simple Profile MPEG-4 streams. These instructions are of three different kinds: get or view a fixed-length bit field, get an individual variable length code and get the DCT coefficients for the whole macroblock. Additionally, the Huffman Decoder provides support for the error-resiliency features of MPEG-4. It can be used to read data-partitioned Video Object Planes, with or without Reversible Variable Length Codes (RVLCs). It cannot, however, read RVLCs backwards.

AC/DC Predictor

If the input stream is MPEG-1 or MPEG-2, the AC/DC predictor passes through. Otherwise, it receives data from the zig-zag through a 19-bit stream interface. A predictor is added to the incoming AC/DC coefficients. The result is saturated and output to the inverse quantizer through a similar interface. This result will also be used as future predictors. For prediction, this block must save an entire macroblock line of informations. This module supports MPEG-4 simple profile.

Inverse Quantizer

The Inverse Quantizer block resides between the AC/DC predictor block and the inverse DCT block. Its primary function is to receive coefficients from the AC/DC predictor, scale them and send them to the IDCT. It supports the MPEG-1, MPEG-2 MP@ML and MPEG-4 simple profile.

Inverse DCT

The IDCT (Inverse Discrete Cosine Transform) module is a hardware implementation of the DCT/IDCT of an 8x8 pixel block used in MPEG compression/ decompression. The DCT transforms a block of 8x8 pixels into a block of 8x8 transformed coefficients. The IDCT transforms a block of 8x8 transformed coefficients back into a block of 8x8 pixels.

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Motion Compensation Module

The Motion Compensation Module performs all the motion compensation tasks required to decode MPEG-1, MPEG-2 and MPEG-4 bitstreams. This includes predicting the image block for the picture being decoded, using pixels from previously decoded pictures.

30. Additional illustrations of known ASIC structures for a decoder can be found, for example, in the datasheet for the Cirrus Logic CS92210 MPEG-2 Video Encoder/Decoder, dated 2001 (Copy attached as Exhibit E to this Declaration); in the datasheet for the Philips SAA7201 Integrated MPEG2 AVG Decoder, dated March 28, 2001 (Copy attached as Exhibit F to this Declaration); and in the datasheet for the SGS-Thomson Microelectronics STi3520 MPEG Audio/MPEG-2 Video Integrated Decoder, dated October 1996 (Copy attached as Exhibit G to this Declaration).

31. An illustration of a known FPGA structure for a decoder can be found, for example, in the datasheet for the Amphion CS6651 MPEG-2 Video Decoder for FPGAs (Copy attached as Exhibit H to this Declaration). This datasheet is dated August 2002. A person of ordinary skill in the art would have appreciated that such decoders were commercially available at that time. As shown on p. 1 of the datasheet, decoders known at the time of the patent application included the basic structural building blocks of entropy decoding (*i.e.*, Variable Length Code Decoder), inverse scanning (*i.e.*, Run Level Decoder), inverse quantization (*i.e.*, Inverse Quantization), inverse transform (*i.e.*, IDCT), and inverse prediction (*i.e.*, Motion Compensation):

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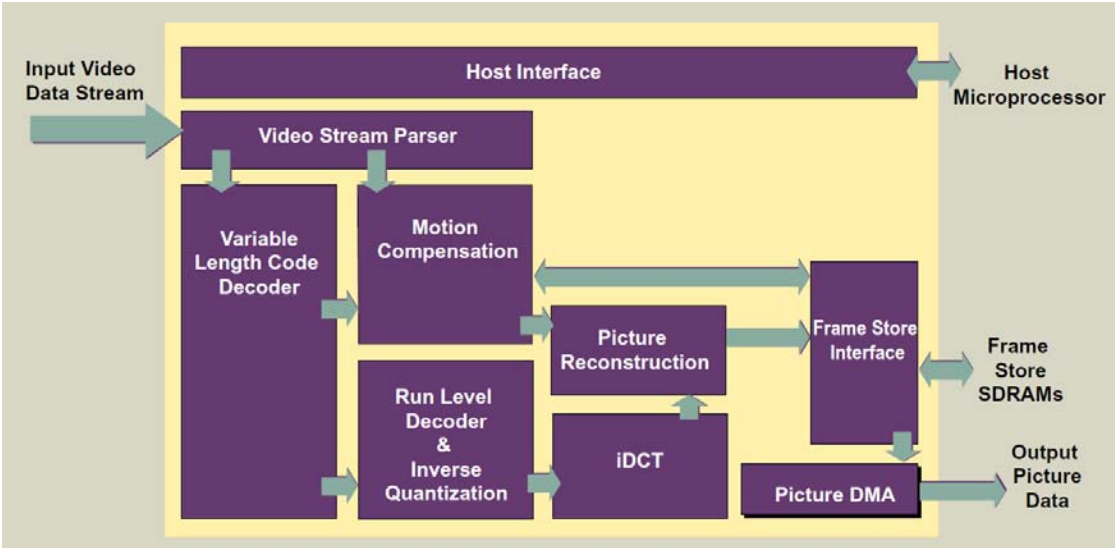

32. An illustration of how these various building blocks were known to those of ordinary skill in the art can be found, for example, in the explanation of each block on p. 2, where these functions are described without further elaboration:

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FUNCTIONAL BLOCK OVERVIEW

VIDEO STREAM PARSER

The Video Stream Parser unit extracts various encoding parameters from the input video stream and any requested user specific data contained within the stream, such as closed-caption or teletext data. This information is contained in headers at each layer of the stream and may be used throughout the rest of the decoding and reconstruction process. Selected user data is stored to buffer space and made available to the host CPU. Having removed header information from the stream, the Video Stream Parser unit passes the variable length encoded picture data to the Variable Length Code (VLC) Decoder unit. A range of parameters describing the overall stream and the picture currently being decoded is made available to the rest of the decoder.

VARIABLE LENGTH CODE DECODER

The Variable Length Code Decoder unit decodes the Huffman- style variable length encoded picture data. The outputs of this unit include the Discrete Cosine Transform (DCT) block run-level information for the Inverse DCT (iDCT) unit and decoded macroblock motion vectors for the motion compensation unit as well as a number of information fields describing the section of the picture currently being decoded. These decoded fields are made available to the rest of the decoder.

RUN-LEVEL DECODER & INVERSE QUANTIZATION

The output run-level information from the VLC decoder is converted into complete blocks of 64 quantized DCT coefficients by the Run-Level decoder. These coefficients are passed to the Inverse Quantizer for conversion back to actual DCT coefficients. To perform this, the Inverse Quantizer keeps track of a number of tables and scale factors, all extracted from the input video stream.

INVERSE DCT

This high performance unit performs the inverse quantization of 8x8 DCT-encoded Y, Cr and Cb pixel blocks. This key unit is capable of streaming data through continuously; transforming every 64 clock cycles an entire block of 8x8 DCT coefficients into an 8x8 block of pixel samples or estimated sample corrections.

MOTION COMPENSATION

Where the video data is encoded as an estimate using previous pictures and a set of corrections, the Motion Compensation unit forms the estimated pixel values. The Motion Compensation unit takes decoded motion vectors from the Variable Length Code Decoder unit and translates them into row and column coordinates within the pictures from which the estimations are being made. The reference samples for these coordinates are requested from the Frame Store Interface and the resulting pixels combined where necessary to form the estimated values for the block being decoded.

PICTURE RECONSTRUCTION

The Picture Reconstruction unit combines decoded pixels or corrections from the iDCT unit with the estimated pixels from the Motion Compensation Unit and writes the resulting pixels to the Frame Store, ready for subsequent display or reference.

FRAME STORE INTERFACE

The Frame Store is required for the storage of the two reference pictures used in the MPEG2 algorithm to form the estimated pixels. It also stores the frame currently being decoded and another frame currently being displayed. This allows the decoding and the display operations to be decoupled making audio/video synchronization simpler to maintain.

33. An illustration of a known DSP structure for a decoder can be found, for example, in the application report entitled *MPEG-2 Video Decoder: TMS320C62x Implementation* by Texas Instruments (Copy attached as Exhibit I to this Declaration). This report is dated March 2000. A person of ordinary skill in the art would have appreciated that such decoders were commercially available at that time. As shown in Figure 1 on p. 3 of the application report, the MPEG-2 Video Decoding Algorithm was known at that time:

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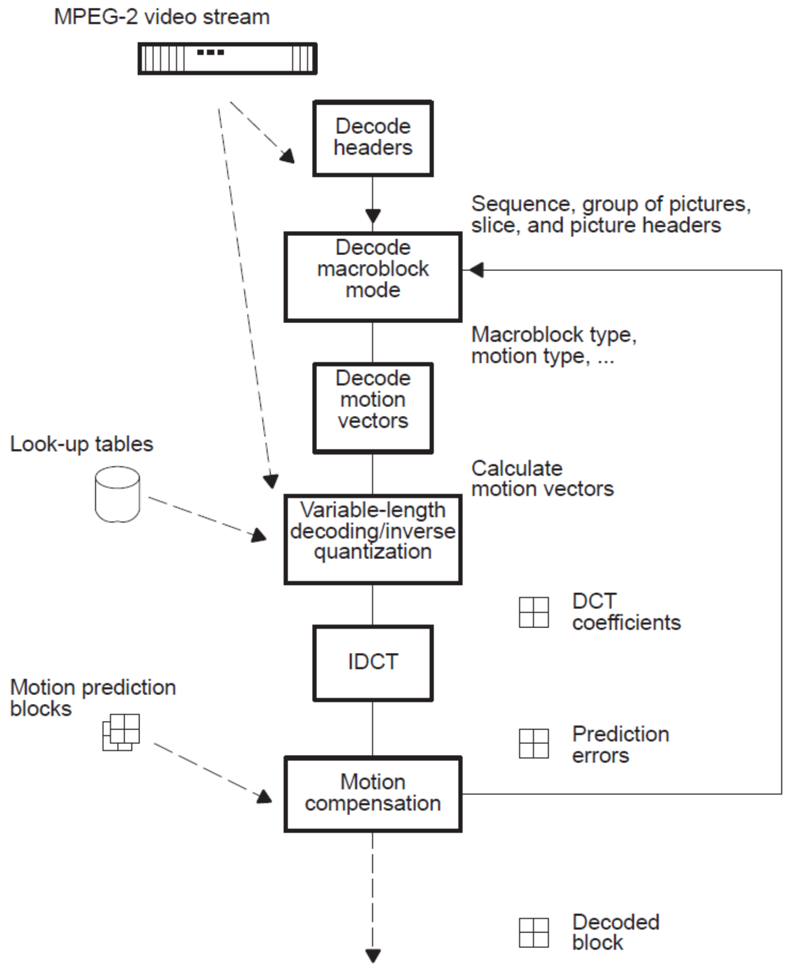

Figure 1. MPEG-2 Video Decoding Algorithm

34. Moreover, a person of ordinary skill in the art appreciated that performing this algorithm involved the use of basic structural building blocks of entropy decoding (*i.e.*, VLD[2]), inverse scanning (*i.e.*, VLD), inverse quantization (*i.e.*, VLD), inverse transform (*i.e.*, IDCT), and inverse prediction (*i.e.*, Motion compensation address calculation; Motion compensation kernel), as shown on pp. 4-5 of the application report:

[2] This application report uses a functional block labeled "VLD" to represent the variable-length coding decoding / inverse quantization block in the flowchart of the MPEG-2 Video Decoding algorithm on p. 3.

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3.2 Decoder Structure

The decoder is divided into the following modules (see Figure 2):

- VLD, which includes functions to perform variable-length decoding, run-length expansion and dequantization
- IDCT, which includes functions to perform inverse discrete cosine transform
- Motion compensation address calculation, which includes functions to calculate the reference blocks location and to fetch the blocks into internal memory
- Motion compensation kernel, which includes functions to calculate the prediction pixels
- Miscellaneous functions to decode header information, motion vectors, etc.
- Implementation of IALG and IRTC interfaces as required in xDAIS

The modules are glued together with the decoder control code. The control code invokes the functions in different modules as well as passes and receives the data.

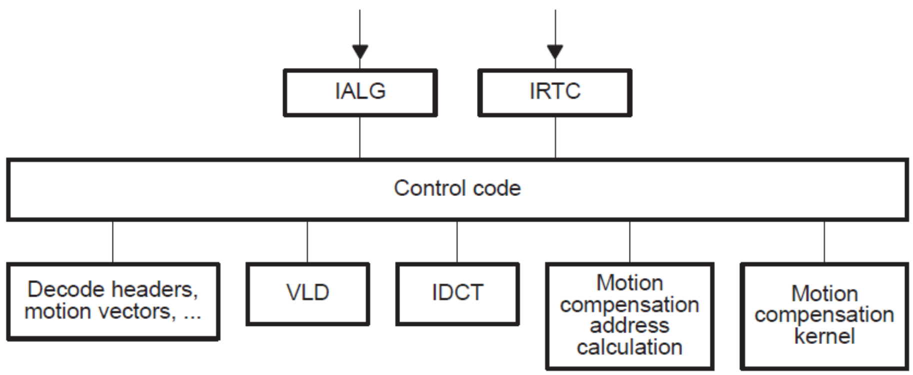

Figure 2. MPEG-2 Video Decoder Structure

35. Additional illustrations of a known DSP structure for a decoder can be found, for example, in the datasheet for the MAP-CA DSP MPEG-4 Video Decoder by Equator Technologies, Inc., dated May 11, 2001 (Copy attached as Exhibit J to this Declaration).

36. An illustration of a known decoder structure using a processor running software can be found, for example, in the paper by Nadehara, et al., *Software MPEG-2 Video Decoder on a 200-MHz, Low-power Multimedia Microprocessor*, IEEE Intl. Conf. ASSP (1998) (Copy attached as Exhibit K to this Declaration). As shown on p. 3143, decoders known at that time included the basic structural building blocks of entropy decoding and inverse scanning (*i.e.*, Variable Length Decoding (VLD)), inverse quantization (*i.e.*, Inverse Quantization), inverse transform (*i.e.*, IDCT), and inverse prediction (*i.e.*, Motion Compensation):

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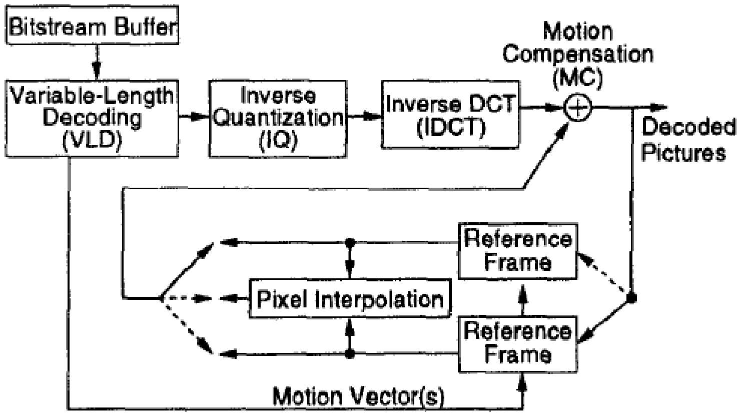

Figure 2: MPEG-2 Video Decoding Process.

37. The Nahendra article describes this software as comprising four procedures:

> The MPEG-2 video decoding process mainly comprises of four procedures as shown in Figure 2; variable length decoding (VLD), inverse quantization (IQ), inverse discrete cosine transform (IDCT), and motion compensation (MC). Nahendra, et al., at p. 3143.

38. The term "CODEC" has arisen in the art in order to refer to a matched encoder/decoder pair, whether implemented in hardware or software. This term is telling in that it emphasizes the strict reciprocity that must prevail between an encoder and a decoder. An example of a hardware CODEC is given by Konstantinides, et al., *Design of an MPEG-2 Codec*, IEEE Signal Processing Magazine, July 2002 (Copy attached as Exhibit L to this Declaration). In fact, the commercial piece part described is usable as either an encoder or a decoder:

> In this section we describe the design and architecture of the CS92288 MPEG-2 a/v codec from Cirrus Logic. This is a half-duplex (that is, it either encodes or decodes), MPEG-2, MP@ML, audio and video codec with programmable system multiplexor and demultiplexor and OSD. Konstaninedes, et al, at p. 36.

The reciprocal relationship between the encoder and the decoder is borne out by the fact that the single chip serves both purposes.

39. Regardless of implementation, known digital video decoders decoded an encoded picture *one* macroblock at a time in frame coding mode or field coding mode. This was a common feature of digital video decoders because they were required by video coding standards to

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recognize pictures encoded as macroblocks. The specification of the Motorola Patents describes an improvement to the known single-macroblock AFF coding techniques by coding pictures a macroblock *pair* at a time in frame coding mode or field coding mode.

40. A person of ordinary skill would therefore have no difficulty understanding from the disclosure of the '374 patent that a decoder is the identified structure for performing the function in claim 14 of the '374 patent of "decoding at least one of a plurality of smaller portions at a time of the encoded picture that is encoded in frame coding mode and at least one of said plurality of smaller portions at a time of the encoded picture in field coding mode."

41. Likewise, a person of ordinary skill would understand from the disclosure of the '375 patent that a decoder is the structure for performing the function in claim 13 of the '375 patent of "selectively decoding at least one of a plurality of smaller portions at a time of the encoded picture that is encoded in frame coding mode and at least one of said plurality of smaller portions at a time of the encoded picture in field coding mode."

42. In addition, a person of ordinary skill in the art would understand from the disclosure of the '376 patent that a decoder is the structure for performing the function in claim 22 of the '376 patent of "decoding at least one of a plurality of processing blocks at a time, each processing block containing a pair of macroblocks or a group of macroblocks, each macroblock containing a plurality of blocks, from said encoded picture that is encoded in frame coding mode and at least one of said plurality of processing blocks at a time that is encoded in field coding mode."

43. Claim 14 of the '374 patent and Claim 13 of the '375 patent also require that the "apparatus for decoding" include "means for using said plurality of decoded smaller portions to construct a decoded picture." Claim 22 of the '376 patent requires that the "apparatus for decoding" includes "means for using said plurality of decoded processing blocks to construct a decoded picture."

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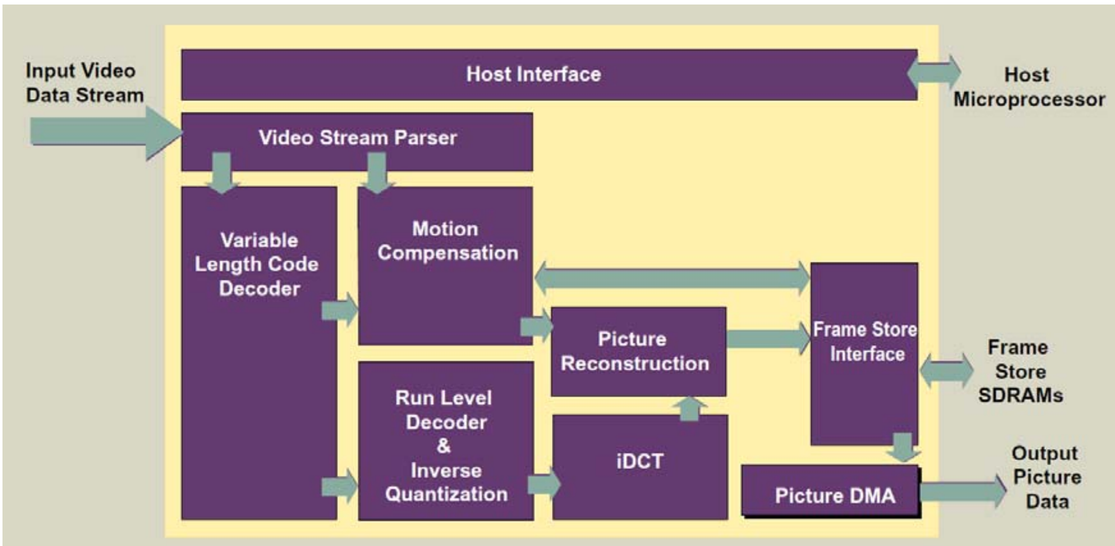
44. Reconstructing a picture using decoded parts of an encoded picture is a common feature of digital video decoders because decoders are required by video coding standards to reconstruct pictures encoded in parts.

45. For example, the Amphion CS6651 MPEG-2 Video Decoder for FPGAs (Ex. H) included the basic structural building block of picture reconstruction ("Picture Reconstruction"), as shown on page one of the datasheet:



46. An illustration of how well-known the picture reconstruction structural building block was to those of ordinary skill in the art is illustrated, for example, in the explanation of it on p. 2 of the datasheet:

PICTURE RECONSTRUCTION

The Picture Reconstruction unit combines decoded pixels or corrections from the iDCT unit with the estimated pixels from the Motion Compensation Unit and writes the resulting pixels to the Frame Store, ready for subsequent display or reference.

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47. Another illustration of a known structure for a decoder can be found in Takata, et al., *The D30V/MPEG Multimedia Processor*, IEEE Micro July-August 1999 (Copy attached as Exhibit M to this Declaration). Figure 1 of Takata shows a block diagram of the MPEG-2 video and audio decoder that includes picture reconstruction ("Reconstruction"):

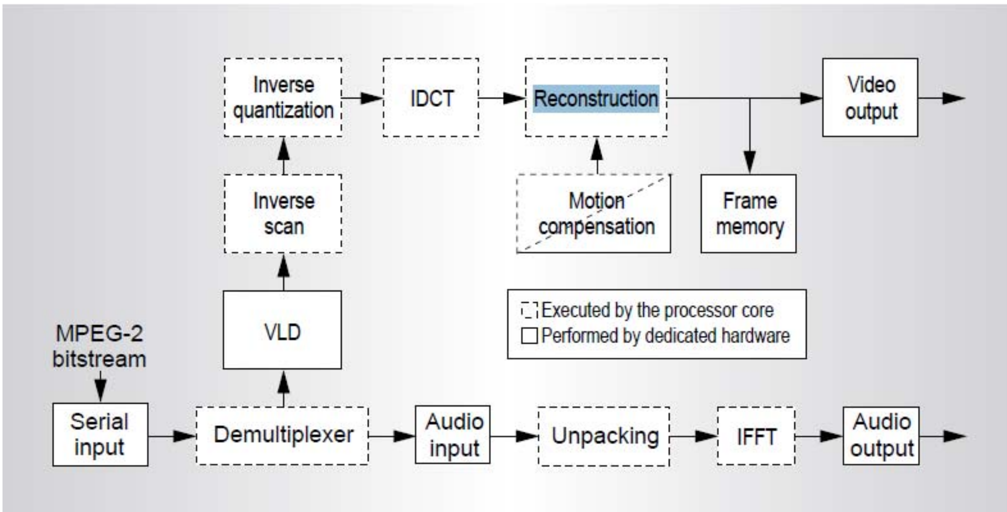

Figure 1. MPEG-2 video and audio decoding.

48. As shown in Figure 1 of Takata, the blocks with hashed borders are implemented as software on a processor, whereas the blocks with solid lines are implemented in dedicated hardware. Thus, the decoder structure of Takata is a hybrid of an ASIC and a processor executing software code.

49. In view of the foregoing, a person of ordinary skill would have no difficultly understanding from the disclosure of the '374 patent that a decoder is the identified structure for performing the function in claim 14 of the '374 patent of "using said plurality of decoded smaller portions to construct a decoded picture."

50. Likewise, a person of ordinary skill would understand from the disclosure of the '375 patent that a decoder is the structure for performing the function in claim 13 of the '375 patent of "using said plurality of decoded smaller portions to construct a decoded picture."

51. In addition, a person of ordinary skill in the art would understand from the disclosure

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of the ‘376 patent that a decoder is the structure for performing the function in claim 22 of the ‘376 patent of “using said plurality of decoded processing blocks to construct a decoded picture.”

52. Where the claimed apparatuses differed from known decoder structures for decoding digital video, those differences are described in the specification, as discussed below with respect to the algorithms. In particular, a person of ordinary skill in the art would have known how to modify the known structural building blocks of a decoder (including prediction) to operate on macroblock pairs in frame mode and field mode, as set forth in the specification.

V. DISCLOSURE OF ALGORITHM FOR “MEANS FOR [SELECTIVELY] DECODING” IN THE SPECIFICATION

53. Where the claimed apparatuses differed from known decoder structures for decoding digital video, those differences are described in the specification.

54. With respect to the ‘374 patent, a person of ordinary skill in the art reading the “means for decoding ... in inter coding mode” would understand that the claim element is directed to using inter prediction to decode pairs of macroblocks that are in frame mode or in field mode, and that the specification describes the algorithm for doing so. A person of ordinary skill would have understood this because this claim element refers specifically to “inter coding mode.”

55. The specification describes the algorithm for performing inter coding on macroblock pairs that are in frame mode or in field mode. *See, e.g.*, ‘374 patent, 9:16-12:56. For example, the specification describes a decoder. *Id.* at 2:9-19, 4:57-5:3. The specification describes how the decoder receives from a bitstream information including pairs of macroblocks and a frame/field flag before each macroblock pair that indicates which mode, frame mode or field mode, is used in coding the macroblock pair. *Id.* at 8:46-65, Fig. 11, Fig. 7. The specification further describes how the decoder performs inter prediction on blocks of the macroblock pairs in frame mode and field mode. *Id.* at 2:20-41, 5:4-44, 9:9-12:56, Fig. 12, Fig. 7, 7:50-53, 7:65-67. The specification describes how the decoder uses one of the median, average, weighted average (*Id.* at 9:54-59), “yes/no method” (*Id.* at 9:60-10:3), the “always method” (*Id.* at 10:4-14), the “selective method”

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(*Id*. at 10:15-11:27), the "alt selective method" (*Id.* at 11:28-12:17), or "directional segmentation prediction" (*Id.* at 12:18-56).

56. A person of ordinary skill in the art would understand from the specification that the disclosure of a frame/field flag is linked to the claimed function of decoding macroblock pairs together in frame coding mode and field coding mode. For example, the specification describes how the frame/field flag indicates which mode, frame or field, the macroblock pair is in. '374 patent, 8:46-69 ("...a frame/field flag bit is preferably included in a picture's bitstream to indicate which mode, frame mode or field mode, is used..."), 8:55-58 ("If the AFF is performed on pairs of macroblocks, the frame/field flag (112) is preferably included before each pair of macroblock in the bitstream.").

57. A person of ordinary skill in the art would understand that that the various inter prediction methods disclosed in the specification are linked to the claimed function of decoding macroblock pairs together in frame coding mode and field coding mode. For example, the specification describes inter prediction in the context of macroblock pairs in frame mode and field mode. '374 patent, 9:46-59 (the blocks "can be in either frame or field mode"), 10:34-37 (referring to "macroblock pair based AFF"), 11:28-31 ("[t]his method can be used in ... pair based macroblock AFF coding").

58. A person of ordinary skill in the art would further understand from the specification that prediction (both inter and intra) is a frame/field **decoding** operation (where prediction is performed on blocks of macroblock pairs in frame/field mode), not an operation that occurs after frame/field decoding. *See e.g.*, '374 patent, 15:64-65 ("In the case of decoding the prediction modes of blocks . . ."), 16:1-2 ("[I]n the case of decoding the prediction modes of blocks . . ."), 16:4-5 ("In the case of decoding the prediction mode of blocks . . ."), 16:6-7 ("In the case of decoding the prediction modes of the block . . ."), 15:49-50 ("blocks ... in frame or field mode"), 16:12-23, **(**"macroblock pair (170) is decoded in field mode . . ."), 16:24-35 **(**"macroblock pair

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(170) is decoded in frame mode . . ."), 10:34-37 (referring to "macroblock pair based AFF"), 11:28-31 ("[t]his method can be used in ... pair based macroblock AFF ... coding").

59. Based on this disclosure, a person of ordinary skill in the art would understand the algorithm performed by the decoder to be:

> (1) receives from a bitstream information including pairs of macroblocks and a frame/field flag before each macroblock pair that indicates which mode, frame mode or field mode, is used in coding the macroblock pairs; and (2) performs inter prediction on blocks of the macroblock pairs in frame mode and field mode using at least one of the median, average, weighted average, "yes/no method," "always method," "selective method," "alt selective method," or "directional segmentation prediction."

60. A person of ordinary skill, having read the specification, would understand how to write software to perform that algorithm if the decoder were implemented using a processor.

61. With respect to the '375 patent, a person of ordinary skill in the art reading the "means for decoding ... in intra coding mode at a time" would understand that the claim element is directed to using intra prediction to decode pairs of macroblocks that are in frame mode or in field mode, and that the specification describes the algorithm for doing so. A person of ordinary skill would have understood this because this claim element refers specifically to "intra coding mode."

62. The specification describes the algorithm for performing intra coding on macroblock pairs. *See, e.g.*, '374 patent, 14:37-16:63. For example, the specification describes a decoder. *Id.* at 1:59-67, 2:9-19, 4:57-5:3. The specification describes how the decoder receives from a bitstream information including pairs of macroblocks and a frame/field flag before each macroblock pair that indicates which mode, frame mode or field mode, is used in coding the macroblock pair. *Id.* at 8:46-65, Fig. 11, Fig. 7. The specification further describes how the decoder performs intra prediction on blocks of the macroblock pairs in at least one of the vertical, horizontal, DC prediction, diagonal down/left, diagonal down/right, vertical-left, horizontal-down, vertical-right, horizontal-up, or plane prediction modes, *Id.* at 14:46-63. The specification further

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describes how neighboring blocks A and B are determined by at least one of Rule 1, Rule 2, Rule 3, or Rule 4. *Id.* at 15:50-16:63, FIGs. 17a-d.

63. As discussed in ¶ 56 above, a person of ordinary skill in the art would understand from the specification that the disclosure of a frame/field flag is linked to the claimed function of decoding macroblock pairs together in frame coding mode and field coding mode.

64. As discussed in ¶ 58 above, a person of ordinary skill in the art would understand from the specification that prediction is a frame/field **decoding** operation, not an operation that occurs after frame/field decoding.

65. A person of ordinary skill in the art would understand from the specification that the various intra prediction methods disclosed in the specification are linked to the claimed function of decoding macroblock pairs together in frame coding mode and field coding mode. For example, the specification describes intra prediction in the context of macroblock pairs in frame mode and field mode. *See, e.g.*, '374 patent, 14:64-15:3 ("An intra block and its neighboring blocks may be coded in frame or field mode."), 15:48-49 ("Block C and its neighboring blocks A and B can be in frame or field mode"), 15:64-65 ("In the case of decoding the prediction modes of blocks . . ."), 16:12-23, **(**"If the above macroblock pair (170) is decoded in field mode . . ."), 16:24-35 **(**"if the above macroblock pair (170) is decoded in frame mode . . .").

66. Based on this disclosure, a person of ordinary skill in the art would understand the algorithm performed by the decoder to be:

> (1) receives from a bitstream information including pairs of macroblocks and a frame/field flag before each macroblock pair that indicates which mode, frame mode or field mode, is used in coding the macroblock pairs; and (2) performs intra prediction on blocks of the macroblock pairs in at least one of the vertical, horizontal, DC prediction, diagonal down/left, diagonal down/right, vertical-left, horizontal-down, vertical-right, horizontal-up, or plane prediction modes, using neighboring blocks determined by at least one of Rule 1, Rule 2, Rule 3 or Rule 4 at col. 15:52-16:63.

67. A person of ordinary skill, having read the specification, would understand how to write software to perform that algorithm if the decoder were implemented using a processor.

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68. With respect to the '376 patent, a person of ordinary skill in the art reading the "means for decoding ... in a horizontal scanning path or a vertical scanning path" would understand that the claim element is directed to using a horizontal scanning path or a vertical scanning path to decode pairs of macroblocks, and that the specification describes the algorithm for doing so. A person of ordinary skill would have understood this because this claim element refers specifically to a "horizontal scanning path" and a "vertical scanning path."

69. The specification describes the algorithm for performing decoding in a horizontal or vertical scanning path. *See, e.g.*, '374 patent, 8:1-18. For example, the specification describes a decoder. *Id.* at 1:59-67, 2:9-19, 4:57-5:3. The specification describes that the decoder receives from a bitstream information including pairs of macroblocks and a frame/field flag before each macroblock pair that indicates which mode, frame mode or field mode, is used in coding the macroblock pair. *Id.* at 8:46-65, Fig. 11, Fig. 7. The specification further describes that the decoder decodes the macroblock pairs of a picture from left to right and from top to bottom, as shown in FIG. 9 path 900, *or* from top to bottom and from left to right, as shown in FIG. 9 path 901. *Id.* at FIG. 9, 8:1-14. The specification further describes that the decoder, within each frame macroblock pair, decodes the top macroblock of the macroblock pair first, followed by the bottom macroblock, and within each field macroblock pair decodes the top field macroblock of the macroblock pair first, followed by the bottom field macroblock. *Id.* at FIG. 9, 8:14-18.

70. As discussed in ¶ 56 above, a person of ordinary skill in the art would understand from the specification that the disclosure of a frame/field flag is linked to the claimed function of decoding macroblock pairs together in frame coding mode and field coding mode.

71. As discussed in ¶ 58 above, a person of ordinary skill in the art would understand from the specification that prediction is a frame/field **decoding** operation, not an operation that occurs after frame/field decoding.

72. Based on this disclosure, a person of ordinary skill in the art would understand the algorithm performed by the decoder to be:

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> (1) receives from a bitstream information includ*ing* pairs of macroblocks and a frame/field flag before each macroblock pair that indicates which mode, frame mode or field mode, is used in coding the macroblock pairs; (2) decodes the macroblock pairs of a picture from left to right and from top to bottom, as shown in FIG. 9 path 900, or from top to bottom and from left to right, as shown in FIG. 9 path 901; and (3) within each frame macroblock pair decodes the top macroblock of the macroblock pair first, followed by the bottom macroblock, and within each field macroblock pair decodes the top field macroblock of the macroblock pair first, followed by the bottom field macroblock.

73. A person of ordinary skill, having read the specification, would understand how to write software to perform that algorithm if the decoder were implemented using a processor.

74. Finally, a person of ordinary skill in the art would understand that the algorithm for the "means for decoding" elements would ***not*** include re-interleaving the lines of a field macroblock pair. Microsoft refers to this process as "frame/field decoding." ECF No. 205 at 11. Re-interleaving the lines of a field macroblock pair is the reverse of Figure 8 of the Motorola Patents. Figure 8 illustrates to one of ordinary skill in the art that in the encoding direction (from left to right), the encoder splits the odd and even lines of the pair of frame macroblocks to form top and bottom field macroblocks. A person of ordinary skill in the art understands that, in the decoding direction, the decoder operates in reverse (i.e., from right to left)—the top and bottom field macroblocks depicted on the right in FIG. 8 are re-interleaved to construct the pair of frame macroblocks depicted on the left of FIG. 8. As Microsoft acknowledges, the re-interleaving occurs after the "inverse prediction" block shown on slide 29 of Motorola's Markman tutorial. ECF No. 205 at 11. Hence, a person of ordinary skill in the art would appreciate that the re-interleaving occurs after the function claimed in the "means for decoding," and is therefore part of the function claimed in the "means for using" (described in detail below).

VI. DISCLOSURE OF ALGORITHM FOR "MEANS FOR USING" IN THE SPECIFICATION

75. Where the claimed apparatuses differed from known decoder structures for decoding digital video, those differences are described in the specification.

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76. With respect to the Motorola Patents, a person of ordinary skill in the art reading the "means for using" would understand that the claim element is directed to "using said plurality of decoded [smaller portions / processing blocks] to construct a decoded picture." The specification describes the algorithm for constructing a decoded picture using decoded macroblock pairs. *See, e.g.*, '374 patent, 7:25-67, 8:46-65. For example, the specification describes a decoder. *Id.* at 2:9-19, 4:57-5:3. The specification describes that, for a decoded frame macroblock pair, the decoder uses the frame macroblocks of the macroblock pair for the decoded picture. *Id.* at FIG. 7, 7:44-48. The specification further describes that, for a decoded field macroblock pair, the decoder reinterleaves the top and bottom field lines of the macroblock pair to form frame macroblocks and uses the frame macroblocks of the macroblock pair for the decoded picture. *Id.* at FIGs. 7 and 8, 7:54-65. The specification further describes that, for a frame or field macroblock pair in which a macroblock is skipped, the decoder uses a co-located macroblock in a reference picture for the decoded picture. *Id.* at 12:67-13:5, 13:12-19, 14:21-28.

77. Based on this disclosure, a person of ordinary skill in the art would understand the algorithm performed by the decoder to be:

> (1) for a decoded frame macroblock pair, uses the frame macroblocks of the macroblock pair for the decoded picture; (2) for a decoded field macroblock pair, reinterleaves the top and bottom field lines of the macroblock pair to form frame macroblocks and uses the frame macroblocks of the macroblock pair for the decoded picture; and (3) for a frame or field macroblock pair in which a macroblock is skipped, uses a co-located macroblock in a reference picture for the decoded picture.

78. A person of ordinary skill, having read the specification, would understand how to write software to perform that algorithm if the decoder were implemented using a processor.

79. A person of ordinary skill in the art would understand that the algorithm for the "means for using" includes re-interleaving the lines of a field macroblock pair. Microsoft refers to this process as "frame/field decoding." ECF No. 205 at 11. This process is the reverse of Figure 8 of the Motorola Patents. Figure 8 illustrates to one of ordinary skill in the art that in the encoding direction (from left to right), the encoder splits the odd and even lines of the pair of frame

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macroblocks to form top and bottom field macroblocks. A person of ordinary skill in the art understands that, in the decoding direction, the decoder operates in reverse (i.e., from right to left)—the top and bottom field macroblocks depicted on the right in FIG. 8 are re-interleaved to construct the pair of frame macroblocks depicted on the left of FIG. 8. As Microsoft acknowledges, this process occurs after the "inverse prediction" block shown on slide 29 of Motorola's Markman tutorial. ECF No. 205 at 11. Hence, a person of ordinary skill in the art would appreciate that the re-interleaving occurs after the function claimed in the "means for decoding," and is therefore part of the function claimed in the "means for using."

80. A person of ordinary skill in the art would not understand the algorithm for the "means for using" to be "assembling a decoded picture using the decoded [smaller portion/processing blocks] like bricks in a wall." A person of ordinary skill in the art understands from the specification that the "means for using" can also perform copying of skipped macroblocks. '374 patent, 12:67-13:5, 13:12-19, 14:21-28. A person of ordinary skill in the art would therefore understand an algorithm that involves only "assembling ... like bricks in a wall" to be overly narrow.

I declare under penalty of the laws of perjury that, to the best of my knowledge, information and belief, the foregoing is true and correct.

DATED this 6th day of April, 2012, at Petaluma, California.

Timothy J. Drabik

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CERTIFICATE OF SERVICE

I hereby certify that on this day I electronically filed the foregoing with the Clerk of the Court using the CM/ECF system which will send notification of such filing to the following:

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