I hereby certify that this correspondence is being filed using EFS-Web addressed to: Mail Stop Inter Partes Reexam, Central Reexamination Unit, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date shown below.

Dated: February 17, 2011 Signature: /Robert T. Neufeld/
Robert T. Neufeld, Reg. No. 48,394

Docket No. 13557.112021
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Reexamination of:

Lars Bak et al.

Patent No.: 6,910,205

Issue Date: June 21, 2005

For: INTERPRETING FUNCTIONS UTILIZING A HYBRID OF VIRTUAL AND NATIVE MACHINE INSTRUCTIONS

Control No.: Not yet Assigned

Examiner: Not Yet Assigned

Art Unit: Not Yet Assigned

REQUEST FOR *INTER PARTES* REEXAMINATION UNDER 37 C.F.R. § 1.915

Mail Stop Inter Partes Reexam
Attn: Central Reexamination Unit
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

King & Spalding LLP (hereinafter, "Requester") submits, under the provisions of 37 C.F.R. § 1.902 *et seq.*, a Request for Reexamination (hereinafter, "Request") of claims 1-4 and 8 of U.S. Patent No. 6,910,205 (hereinafter, "the '205 patent") entitled "Interpreting Functions Utilizing a Hybrid of Virtual and Native Machine Instructions," issued to Lars Bak et al. on June 21, 2005. A copy of the '205 patent is provided as Exhibit 1 to this Request.

In support of its request, Requester provides the following:

- The $8,800.00 fee for requesting *inter partes* reexamination set forth in 37 C.F.R. § 1.20(c)(2) (37 C.F.R. § 1.915(a));

- An identification of the patent by patent number and every claim for which reexamination is requested (37 C.F.R. § 1.915(b)(1));

- A citation of the patents and printed publications which are presented to provide a substantial new question of patentability (37 C.F.R. § 1.915(b)(2));

- A statement pointing out each substantial new question of patentability based on the cited patents and printed publications, and a detailed explanation of the pertinency and manner of applying the patents and printed publications to every claim for which reexamination is requested (37 C.F.R. § 1.915(b)(3));

- A copy of every patent or printed publication relied upon or referred to in paragraphs (b)(1) through (3) of 37 C.F.R. § 1.915, accompanied by an English language translation of all the necessary and pertinent parts of any non-English language document (37 C.F.R. § 1.915(b)(4));

- A copy of the entire patent including the front face, drawings, and specification/claims (in double column format) for which reexamination is requested, and a copy of any disclaimer, certificate of correction, or reexamination certificate issued in the patent. All copies must have each page plainly written on only one side of a sheet of paper (37 C.F.R. § 1.915(b)(5));

- A certification by the third party requester that a copy of the request has been served in its entirety on the patent owner at the address provided for in 37 C.F.R. § 1.33(c). The name and address of the party served must be indicated. If service was not possible, a duplicate copy of the request must be supplied to the Office (37 C.F.R. § 1.915(b)(6));

- A certification by the third party requester that the estoppel provisions of 37 C.F.R. § 1.907 do not prohibit the inter partes reexamination (37 C.F.R. § 1.915(b)(7)); and

- A statement identifying the real party in interest to the extent necessary for a subsequent person filing an inter partes reexamination request to determine whether that person is a privy (37 C.F.R. § 1.915(b)(8)).

Pursuant to 35 U.S.C. § 303, the prior art references discussed in this Request raise "substantial new questions of patentability" with respect to claims 1-4 and 8 of the '205 patent.

Pursuant to 37 C.F.R. §§ 1.915(b)(7) and (b)(8), Requester identifies the real party in interest to this third-party request as Google Inc. Requester and the real party in interest further certify that the estoppel provisions of 37 C.F.R. § 1.907 do not prohibit this *inter partes* reexamination.

TABLE OF CONTENTS

I. INTRODUCTION

Requester requests reexamination of claims 1-4 and 8 of U.S. Patent No. 6,910,205 ("the '205 patent") under 35 U.S.C. §§ 311-318 and 37 C.F.R. § 1.903 *et seq*. The application for the '205 patent was filed on July 12, 2002. The '205 patent is assigned to Sun Microsystems, Inc. by virtue of the assignment recorded against U.S. Patent Application No. 08/884,856 to which the '205 patent claims priority.

Substantial new questions of patentability exist with respect to claims 1-4 and 8 of the '205 patent based on references and combinations detailed hereinafter, which were not before the Patent Office during original examination of the '205 patent. The '205 patent is generally directed to generating a new virtual machine instruction that references native instructions (*see, e.g.,* '205 patent, claims 1 and 8); and (a) executing the new virtual machine instruction instead of an original virtual machine instruction (*see, e.g.,* '205 patent, claim 1), or (b) executing the new virtual machine instruction after compiling of the function (*see, e.g.,* '205 patent, claim 8). The claims of the '205 patent were allowed based on the Examiner's conclusion that the single prior art reference applied during prosecution did not disclose limitations (a) or (b) listed above.

However, these very elements, along with all the other limitations of claims 1-4 and 8 of the '205 patent, are disclosed in multiple prior art references that were not before the Examiner at the time of allowance and which form the specific proposed rejections of this Request. Based on the specific proposed rejections discussed herein, this Request raises substantial new questions of patentability with respect to claims 1-4 and 8 of the '205 patent.

More specifically, Requester has identified herein nine (9) prior art patents and printed publications that individually anticipate or, in combination, render obvious each of claims 1-4 and 8 of the '205 patent and thus raise substantial new questions of patentability with respect to these claims of the '205 patent. Eight of these prior art patents and printed publications were

neither cited to, nor considered by, the Examiner during prosecution of the '205 patent and are not cumulative to information cited to or considered by the Examiner during prosecution of the '205 patent. These eight prior art patents and printed publications each anticipate each element of claims 1-4 and 8 of the '205 patent. Only one prior art reference, the Walters '593 patent, was considered by the Examiner during prosecution of the '205 patent. However, the eight new references cited herein cure the alleged disclosure deficiencies identified by the Examiner for the Walters '593 patent, and accordingly, the various combinations of the Walters '593 patent and the eight new references cited herein further render obvious each of claims 1-4 and 8 of the '205 patent.

Accordingly, in view of these listed prior art references and the substantial new questions of patentability raised thereby, Requester respectfully requests the issuance of an order for reexamination of the '205 patent and further requests cancellation of claims 1-4 and 8 of the '205 patent.

II. STATEMENT UNDER 37 C.F.R. § 1.915(B)(3) POINTING OUT SUBSTANTIAL NEW QUESTIONS OF PATENTABILITY

The prior art references discussed herein raise substantial new questions of patentability for claims 1-4 and 8 of the '205 patent.

Section II.A provides an overview of the '205 patent.

Section II.B summarizes certain aspects of the law regarding reexamination.

Section II.C summarizes the evidentiary standards applicable to reexamination.

Section II.D provides a list of all prior art patents and printed publications relied upon in this Request.

Section II.E provides a list of other supporting documents discussed in this Request.

Section II.F provides a summary of pending litigation involving the '205 patent.

Section II.G provides admissions by the Patent Owner of the '205 patent.

Section II.H provides an identification of the substantial new questions of patentability raised in this Request.

Section II.I provides an overview of the substantial new questions of patentability raised in this Request.

A. Overview of the '205 Patent

The '205 patent seeks to increase the execution speed of virtual machine instructions for a function by compiling a portion of the virtual machine instructions of the function into native machine instructions. '205 patent, Abstract. Execution of the native machine instructions may be accomplished by overwriting an original virtual machine instruction of the function with a new virtual machine instruction that specifies execution of the native machine instruction. *Id.* The new virtual machine instruction is thereafter executed instead of the original virtual machine instruction. *Id.* at 8:27-30.

In operation, a selected portion of the virtual machine instructions of the function is compiled into native machine instructions. *Id.* at 7:1-2. A new virtual machine instruction replaces or overwrites an original virtual machine instruction of the selected portion of the function. *Id.* at 7:26-28. The new virtual machine instruction specifies the subsequent execution of the native machine instructions. *Id.* at 7:23-26. When an interpreter executes the virtual machine instructions, the interpreter looks up the native machine instructions specified by executing the new virtual machine instruction instead of the original virtual machine instruction and then executes the native machine instructions. *Id.* at 8:27-30.

The claims of the '205 patent relate to a method for "increasing the execution speed of virtual machine instructions. '205 patent, claims 1 and 8. Claims 1 and 8 are the independent claims at issue in the Request.

Claim 1 recites:

> 1. In a computer system, a method for increasing the execution speed of virtual machine instructions at runtime, the method comprising:
> receiving a first virtual machine instruction;
> generating, at runtime, a new virtual machine instruction that represents or references one or more native instructions that can be executed instead of said first virtual machine instruction; and
> executing said new virtual machine instruction instead of said first virtual machine instruction.

Claim 8 recites:

> 8. In a computer system, a method for increasing the execution speed of virtual machine instructions, the method comprising:
> inputting virtual machine instructions for a function;
> compiling a portion of the function into at least one native machine instruction so that the function includes both virtual and native machine instruction; [and]
> representing said at least one native machine instruction with a new virtual machine instruction that is executed after the compiling of the function.

The '205 patent issued from U.S. Patent Application No. 10/194,040 ("the '040 application"), filed July 12, 2002. The following is a summary of the pertinent portions of the prosecution file history for the '040 application.

As originally filed, the '040 application included claims 1-31, of which claims 1, 11, and 22 were independent claims. The Patent Office issued a first Office Action on the merits on March 5, 2004, rejecting claims 1-31 based on a "same invention" double patenting rejection in view of prior U.S. Patent No. 6,513,156 and rejecting claims 1, 8-12, 19-22, and 29-31 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 5,768,593 to Walters (hereinafter, "the Walters '593 patent").

The applicant filed a response to the March 5, 2004 Office Action on May 27, 2004, canceling claims 13-20 and 23-28, adding claims 32-41 (with claims 32, 33, and 34 being independent), and amending claims 1 and 2. Thus, claims 1-12, 21-22, and 29-41 were pending in the '040 application, with claims 1, 11, and 31-34 being independent. New claims 32 and 33 eventually resulted in patented claims 1 and 8 of the '205 patent, respectively. With regard to claims 32 and 33, the applicant argued that Walters does not teach or suggest the following: a new virtual machine instruction that represents or references one or more native instructions that can be executed instead of a first virtual machine instruction (claim 32); and representing at least one native machine instruction with a virtual machine instruction that is executed after compiling the function (claim 33). *See* Response dated May 27, 2004, at p. 12.

On September 23, 2004, the Patent Office issued a final Office Action, rejecting claims 1-12, 21-22, and 29-41 (all pending claims) based on an obviousness-type double patenting rejection in view of prior U.S. Patent No. 6,513,156 and rejecting claims 1, 8-12, 29-31, 33-36, and 38-41 under 35 U.S.C. § 102(e) as being anticipated by the Walters '593 patent.

The applicant filed a response to the September 23, 2004 Office Action on October 7, 2004, including a terminal disclaimer to overcome the double patenting rejection and canceling claims 1 and 8-31 without amending any claims. Thus, claims 2-7 and 32-41 were pending in the '040 application, with claims 32-34 being independent. The applicant did not address the patentability of any claims in view of the Walters '593 patent.

The Patent Office issued an Advisory Action on December 14, 2004, withdrawing the double patenting rejection in response to the filed terminal disclaimer and indicating that claims 2-7 and 32 were allowed. Claims 33-41 remained rejected.

After an interview with the Examiner on January 3, 2005, the Examiner withdrew remaining claim rejections based on the Walters '593 patent and issued a Notice of Allowance on January 13, 2005. According to the Examiner in his Statement of Reasons for Allowance:

> The cited prior art of record however, does not teach or allude to the generation of a new virtual instruction that represents the one or more native instructions such that this new instruction is executed either (1) instead of the original virtual instruction [claim 32, corresponding to patented claim 1] or (2) after the compiling of the function [claim 33, corresponding to patented claim 8].

Notice of Allowance dated January 13, 2005, at p. 2.

The applicant paid the issue fee on March 25, 2005, and the Patent Office issued the '205 patent on June 21, 2005.

B. Aspects of the law governing reexamination

1. Citation of prior art

"Any person at any time may file a request for reexamination by the Office of any claim of any patent on the basis of any prior art cited under the provisions of section 301." 35 U.S.C. § 302. Section 301 limits prior art to "patents or printed publications." 35 U.S.C. § 301.

MPEP 2128 classifies a reference as a printed publication if it is accessible to the public:

> A reference is proven to be a 'printed publication' 'upon a satisfactory showing that such *document* has been disseminated or otherwise made available to the extent that persons interested and ordinarily skilled in the subject matter or art, exercising reasonable diligence, can locate it.'

In re Wyer, 655 F.2d 221, 210 USPQ 790 (CCPA 1981) (quoting *I.C.E. Corp. v. Armco Steel Corp.*, 250 F. Supp. 738, 743, 148 USPQ 537, 540 (SDNY 1966)).

2. "Old" prior art can raise a significant new question of patentability

The fact that a prior art reference was cited to or even previously considered by an examiner does not preclude use of that reference to find a substantial new question of patentability ("SNQ"). *See* 35 U.S.C. § 303(a); MPEP Section 2258.01; *see also In re Swanson*,

540 F.3d 1368, 1380-81 (Fed. Cir. 2008) (holding that consideration of a prior art reference in previous litigation and in an original examination does not preclude a finding of a SNQ based on the same prior art reference in reexamination).

A combination of such "old art" and art newly cited during the reexamination proceeding may raise a SNQ. *See* MPEP Section 2258.01. The Patent Office may even find a SNQ based exclusively on previously cited references.

> For example, a SNQ may be based solely on old art where the old art is being presented/viewed in a new light, or in a different way, as compared with its use in the earlier concluded examination(s), in view of a material new argument or interpretation presented in the request.

See id.

3. Obviousness standard under KSR

The Supreme Court recently relaxed the Federal Circuit's requirement of a "teaching/suggestion/motivation test," and instead held that "[t]he combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results." *KSR Int'l Co. v. Teleflex Inc. et al.*, 550 U.S. 398, 416 (2007). The Court noted that "[w]hen a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one. If a person of ordinary skill can implement a predictable variation" of an existing system, then "§103(a) likely bars its patentability." *Id.* at 417. *KSR* also held that "if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious" if within his or her skill. *See id.*

On October 10, 2007, the U.S. Patent and Trademark Office released Examination Guidelines for Determining Obviousness Under 35 U.S.C. 103(a) in View of the Supreme Court

Decision in *KSR Int'l Co. v. Teleflex Inc.*, 72 Fed. Reg. 195 at 57526 (the "PTO Guidelines"). The PTO Guidelines adopt the rationales from the *KSR* decision for determining obviousness. One of the rationales is "'Obvious to Try' – Choosing from a Finite Number of Identified, Predictable Solutions, With a Reasonable Expectation of Success." To reject a claim on this basis, the PTO Guidelines note that pertinent factors to consider are whether "there had been a finite number of identified, predictable potential solutions to the recognized need or problem," and "one of ordinary skill in the art could have pursued the known potential solutions with a reasonable expectation of success." *Id.* at 57532. The PTO Guidelines have been incorporated into the MPEP's examination guidelines for determining obviousness under 35 U.S.C. § 103. *See* MPEP 2141.

Additionally, the Federal Circuit has applied the *KSR* obviousness standard to combine multiple embodiments disclosed in a single prior art reference. *Boston Sci. Scimed, Inc. v. Cordis Corp.*, No. 2008-1073, 2009 U.S. App. LEXIS 588, at *24 (Fed. Cir. Jan. 15, 2009) (holding that a person of ordinary skill would have been motivated to combine one embodiment found in a patent reference with a second, separate embodiment found in the same patent reference.)

4. Prior art references need not be enabling in an obviousness inquiry

Prior art references need not be enabling in the context of an obviousness inquiry. As stated in the MPEP:

> **35 U.S.C. 103(a) REJECTIONS AND USE OF INOPERATIVE PRIOR ART**
>
> "Even if a reference discloses an inoperative device, it is prior art for all that it teaches." *Beckman Instruments v. LKB Produkter AB*, 892 F.2d 1547, 1551, 13 USPQ2d 1301, 1304 (Fed. Cir. 1989). Therefore, "a non-enabling reference may qualify as prior art for the purpose of determining obviousness under 35 U.S.C. 103." *Symbol Techs. Inc. v. Opticon Inc.*, 935 F.2d 1569, 1578, 19 USPQ2d 1241, 1247 (Fed. Cir. 1991).

MPEP 2121.01; *see also* MPEP 2145; *Amgen Inc. v. Hoechst Marion Roussel, Inc.*, 314 F.3d 1313, 1357 (Fed. Cir. 2003) (holding that under 35 U.S.C. § 103, "a reference need not be enabled; it qualifies as prior art, regardless, for whatever is disclosed therein.") (citations to other cases omitted).

5. Claims of the patent are to be broadly construed

In a reexamination proceeding, claims are to be given their broadest construction consistent with the specification. *See In re Icon Health & Fitness, Inc.*, 496 F.3d 1374, 1379 (Fed. Cir. 2007) ("During reexamination, as with original examination, the PTO must give claims their broadest reasonable construction consistent with the specification.").

C. Evidentiary standards

If the prior art patents and printed publications raise a substantial question of patentability of at least one claim of the patent, then a substantial new question of patentability is present. *See* MPEP 2242. A prior art patent or printed publication raises a substantial question of patentability where there is a substantial likelihood that a reasonable examiner would consider the prior art patent or printed publication important in deciding whether or not the claim is patentable. *Id.* In addition to patents and printed publications, admissions by a patentee may also be used as evidence to establish a substantial new question of patentability in combination with a patent or a printed publication. *See* MPEP 2217. An admission by a patentee may reside in a record created during litigation. *See id.* Such patentee admissions may be relied upon for any matter affecting patentability. 37 C.F.R. § 1.205(c)(3).

D. Prior art patents and printed publications relied upon in this Request

In accordance with 37 C.F.R. § 1.915(b)(2), reexamination of claims 1-4 and 8 of the '205 patent is requested in view of the prior art patents and printed publications listed below, which raise substantial new questions of patentability. This Request will demonstrate how

claims 1-4 and 8 of the '205 patent are anticipated and/or rendered obvious in view of the following prior art references:

1. L. Peter Deutsch et al., *Efficient Implementation of the Smalltalk-80 System*, Proceedings of the 11th ACM SIGACT-SIGPLAN Symposium on Principles of Programming Languages, pp. 297-302, 1984 (hereinafter, "Deutsch"), provided as Exhibit 2.

2. David Wakeling, *A Throw-Away Compiler for a Lazy Functional Language*, Fuji International Workshop on Functional and Logic Programming, pp. 287-300, 1995 (hereinafter, "Wakeling"), provided as Exhibit 3.

3. Brian T. Lewis et al., *Clarity MCode: A Retargetable Intermediate Representation for Compilation*, ACM, IR '95, 1/95, San Francisco, California, USA, pp. 119-128, 1995 (hereinafter, "Lewis"), provided as Exhibit 4.

4. Paul Tarau et al., *The Power of Partial Translation: An Experiment with the C-Ification of Binary Prolog*, ACM Symposium on Applied Computing, pp. 152-156, 1995 (hereinafter, "Tarau"), provided as Exhibit 5.

5. Frank Yellin, *The JIT Compiler API*, The JIT Compiler API, October 4, 1996, pp. 1-23 (hereinafter, "Yellin"), provided as Exhibit 6.

6. U.S. Patent No. 6,081,665 to Nilsen et al, entitled "Method for Efficient Soft Real-Time Execution of Portable Byte Code computer Programs," issued on June 27, 2000 from an application filed December 19, 1997 with priority to December 21, 1996 (hereinafter, the "Nilsen '665 patent"), provided as Exhibit 7.

7. U.S. Patent No. 5,842,017 to Hookway et al., entitled "Method and Apparatus for Forming a Translation Unit," issued November 24, 1998 from an application filed January 29, 1996 (hereinafter, the "Hookway '017 patent"), provided as Exhibit 8.

8. Peter Magnusson, *Partial Translation*, Swedish Institute of Computer Science Technical Report (T93.5), Oct. 1993 (hereinafter, "Magnusson"), provided as Exhibit 9.

9. U.S. Patent No. 5,768,593 to Walters et al., entitled "Dynamic Cross-Compilation System and Method," issued June 16, 1998 from an application filed March 22, 1996 (hereinafter, the "Walters '593 patent"), provided as Exhibit 10.

E. Supporting documents discussed in this Request

The following claim charts are provided to assist the Examiner in understanding this Request:

1. Claim Chart based on Deutsch, provided as Exhibit 11.
2. Claim Chart based on Wakeling, provided as Exhibit 12.
3. Claim Chart based on Lewis, provided as Exhibit 13.
4. Claim Chart based on Tarau, provided as Exhibit 14.
5. Claim Chart based on Yellin, provided as Exhibit 15.
6. Claim Chart based on the Nilsen '665 patent, provided as Exhibit 16.
7. Claim Chart based on the Hookway '017 patent, provided as Exhibit 17.
8. Claim Chart based on Magnusson, provided as Exhibit 18.
9. Claim Chart based on the Walters '593 patent, provided as Exhibit 19.
10. *Oracle America, Inc. v. Google Inc.*, Civil Action No.: 3:10-cv-03561-WHA, Oracle America, Inc.'s Preliminary Infringement Contentions for the '205 Patent at Exhibit B-1, provided as Exhibit 20.
11. U.S. Patent Application No. 10/194,040 Prosecution File History, Notice of Allowance dated January 13, 2005, provided as Exhibit 21.

F. Current Litigation

The Requester is aware of at least one current litigation matter involving the '205 patent. On August 12, 2010, Oracle America, Inc. filed a complaint in the U.S. District Court for the Northern District of California alleging that Google Inc. is infringing the '205 patent. The case is styled *Oracle America, Inc. v. Google Inc.*, Civil Action No.: 3:10-cv-03561-WHA (hereinafter, the "Oracle v. Google litigation"). A Joint Case Management Statement for the case provides for a claim construction hearing in the case to take place on April 20, 2011. Fact discovery will end July 29, 2011 and dispositive motions are due September 8, 2011.

G. Patent Owner Admissions

In establishing a substantial new question of patentability, "an admission by the patent owner of record in the file or in a court record may be utilized in combination with a patent or printed publication." MPEP 2217. "Admissions by the patent owner as to any matter affecting patentability may be utilized to determine the scope and content of the prior art in conjunction with patents and printed publications in a prior art rejection, whether such admissions result from patents or printed publications or from some other source." *Id.* (emphasis omitted).

In the Oracle v. Google litigation, the patent owner stated that a pointer in a table that references a native machine instruction is insubstantially different from a new virtual machine instruction. Specifically, with reference to claim 1 of the '205 patent:

> To the extent Android does not literally infringe this claim element, Android contains equivalent elements corresponding to each and every requirement of this claim limitation. When the Android JIT compiles a trace, Android adds the corresponding bytecode instruction counter of the bytecode (the first virtual machine instruction) and a pointer to the compiled trace to the jitEntry table. When interpreting the instruction located at the bytecode instruction counter, Android does a lookup of the bytecode instruction counter in the jitEntry table. If Android finds an entry, Android will execute a branch to the compiled trace instead of executing the bytecode instruction. **The differences, if any, between a "new virtual machine instruction" and an entry in the jitEntry table are insubstantial.** An entry in the jitEntry table (1) performs the same or substantially the same function (direct that native code be executed in place of bytecode) and (2) works in substantially the same way (store a pointer to native code at a location indexed by the bytecode instruction counter) (3) to achieve the same or substantially the same result (faster execution) as this element of the claim.

Oracle America, Inc.'s Preliminary Infringement Contentions for the '205 Patent at Exhibit B-1, pp. 42-43 (emphasis added). Thus, despite the claim language that requires a new virtual machine instruction to be executed instead of an original virtual machine instruction, the patent owner considers a pointer in a table to native code to be substantially the same as the claimed new virtual machine instruction.

H. Identification of Substantial New Questions of Patentability

In this Request, substantial new questions of patentability for claims 1-4 and 8 of the '205 patent are identified in accordance with 37 C.F.R. § 1.915(b)(3) as follows:

1. Anticipation under 35 U.S.C. § 102.

a. Claims 1-4 and 8 are unpatentable under 35 U.S.C. § 102(b) as being anticipated by Deutsch.

b. Claims 1-4 and 8 are unpatentable under 35 U.S.C. § 102(b) as being anticipated by Wakeling.

c. Claims 1-4 and 8 are unpatentable under 35 U.S.C. § 102(b) as being anticipated by Lewis.

d. Claims 1-4 and 8 are unpatentable under 35 U.S.C. § 102(b) as being anticipated by Tarau.

e. Claims 1-4 and 8 are unpatentable under 35 U.S.C. § 102(a) as being anticipated by Yellin.

f. Claims 1-4 and 8 are unpatentable under 35 U.S.C. § 102(e) as being anticipated by the Nilsen '665 patent.

g. Claims 1-4 and 8 are unpatentable under 35 U.S.C. § 102(e) as being anticipated by the Hookway '017 patent.

h. Claims 1-4 and 8 are unpatentable under 35 U.S.C. § 102(b) as being anticipated by Magnusson.

2. Obviousness under 35 U.S.C. § 103(a).

a. Claims 1-4 and 8 are unpatentable under 35 U.S.C. § 103(a) as being obvious over the Walters '593 patent in view of Deutsch.

b. Claims 1-4 and 8 are unpatentable under 35 U.S.C. § 103(a) as being obvious over the Walters '593 patent in view of Wakeling.

c. Claims 1-4 and 8 are unpatentable under 35 U.S.C. § 103(a) as being obvious over the Walters '593 patent in view of Lewis.

d. Claims 1-4 and 8 are unpatentable under 35 U.S.C. § 103(a) as being obvious over the Walters '593 patent in view of Tarau.

e. Claims 1-4 and 8 are unpatentable under 35 U.S.C. § 103(a) as being obvious over the Walters '593 patent in view of Yellin.

f. Claims 1-4 and 8 are unpatentable under 35 U.S.C. § 103(a) as being obvious over the Walters '593 patent in view of the Nilsen '665 patent.

g. Claims 1-4 and 8 are unpatentable under 35 U.S.C. § 103(a) as being obvious over the Walters '593 patent in view of the Hookway '017 patent.

h. Claims 1-4 and 8 are unpatentable under 35 U.S.C. § 103(a) as being obvious over the Walters '593 patent in view of Magnusson.

I. Overview of Substantial New Questions of Patentability

Requester submits that claims 1-4 and 8 of the '205 patent are not patentable over the prior art printed publications and patents discussed herein.

U.S. patent application no. 10/194,040, which matured into the '205 patent, was filed on July 12, 2002. This application was a continuation of U.S. Patent Application No. 08/884,856 filed on June 30, 1997.

Independent claim 1 of the '205 patent is directed to a method for increasing the execution speed of virtual machine instructions at runtime. A first virtual machine instruction is received. A new virtual machine instruction is generated at runtime, where the new virtual machine instruction represents or references one or more native instructions that can be executed instead of the first virtual machine instruction. Then, the new virtual machine instruction is executed instead of the first virtual machine instruction. During prosecution of the '040 application, the Patent Office indicated that independent claim 1 was patentable over the prior art of record (mainly, U.S. Patent No. 5,768,593 to Walters) because the Walters '593 patent allegedly failed to teach executing the new virtual instruction instead of the original virtual instruction. *See* Notice of Allowance dated January 13, 2005, at p. 2, attached hereto as Exhibit 21 (addressing claim 32 of the '040 application, corresponding to patented claim 1 of the '205 patent).

Independent claim 8 is directed to a method for increasing the execution speed of virtual machine instructions. A virtual machine instruction is input for a function. A portion of the function is compiled into at least one native machine instruction so that the function includes both virtual and native machine instructions. At least one native machine instruction is represented with a new virtual machine instruction that is executed after the compiling of the function. During prosecution of the '040 application, the Patent Office indicated that independent claim 8 was patentable over the prior art of record (mainly, the Walters '593 patent) because the Walters '593 patent allegedly failed to teach executing the new virtual instruction after the compiling of the function. *See Id.* (addressing claim 33 of the '040 application, corresponding to patented claim 8 of the '205 patent).

Deutsch: L. Peter Deutsch et al., *Efficient Implementation of the Smalltalk-80 System*, Proceedings of the 11th ACM SIGACT-SIGPLAN Symposium on Principles of Programming Languages, pp. 297-302, 1984 (hereinafter, "Deutsch"), provided as Exhibit 2, is a publication directed to an interactive programming environment in which the same information is represented in more than one way, being converted transparently between representations as needed for efficient use at any moment. Because Deutsch was published in 1983, it is prior art under 35 U.S.C. § 102(b) to the '205 patent, given that the earliest possible priority date for the '205 patent is June 30, 1997. Deutsch was not in front of the Patent Office during the prosecution of the application that matured into the '205 patent, and it is not cumulative to the prior art considered by the Patent Office during the prosecution of the '205 patent.

Deutsch is directed to efficient implementation of the "Smalltalk-80" programming system. *See* Deutsch, Abstract. Optimization techniques for the Smalltalk-80 programming system include representing certain runtime states (both code and data) in more than one form

converting between forms when needed. *See id.* In Deutsch, a virtual machine encounters a virtual instruction that represents a procedure entry point, or procedure call. *See id.* at 298. After translating a procedure in virtual instruction from (e.g., v-code) to its native code form (e.g., n-code), the call to the method-lookup routine is replaced with a call to the address of the newly-generated native code. *See id.* at 299, 300. Thus, the new call instruction (i.e., the call to the method-lookup routine) "represents or references one or more native instructions that can be executed instead of said first virtual machine instruction." *See id.* Then, the "new" call to the address of the newly-generated native code is executed instead of the original call to the method-lookup routine. *See id.*

Deutsch discloses generating a new virtual machine instruction that references native instructions, i.e., creating a new call instruction from a virtual instruction which includes a translated procedure in native code (*see id.* at 298-300) and (a) executing the new virtual machine instruction instead of an original virtual machine instruction, i.e., executing the new call instruction (*see id.*) and (b) executing the new virtual machine instruction after compiling of the function (*see id.* at 299 (describing compilation of the code in v-code, portions of which are translated into n-code)). These limitations, which are disclosed in this prior art reference, form the basis upon which the Patent Office determined the patentability of independent claims 1 and 8 of the '205 patent, respectively.

Deutsch also discloses the remaining limitations of independent claims 1 and 8 and dependent claims 2-4 of the '205 patent. Accordingly, a reasonable examiner would have considered the teachings of Deutsch to be important in determining whether or not the specified claims of the '205 patent were patentable. As set forth in detail in the Claim Chart in Exhibit 11,

Deutsch anticipates claims 1-4 and 8 of the '205 patent. For this reason, Deutsch raises a substantial new question of patentability with respect to claims 1-4 and 8 of the '205 patent.

Wakeling: David Wakeling, *A Throw-Away Compiler for a Lazy Functional Language*, Fuji International Workshop on Functional and Logic Programming, pp. 287-300, 1995 (hereinafter, "Wakeling"), provided as Exhibit 3, is a publication directed to a "throw-away" compiler that creates native code blocks for execution during run time. Because Wakeling was published in 1995, it is prior art under 35 U.S.C. § 102(b) to the '205 patent, given that the earliest possible priority date for the '205 patent is June 30, 1997. Wakeling was not in front of the Patent Office during the prosecution of the application that matured into the '205 patent, and it is not cumulative to the prior art considered by the Patent Office during the prosecution of the '205 patent.

Wakeling discloses translating an X-machine byte code to native code. *See* Wakeling at 291. Wakeling discloses switching between executing X-machine byte code and native code, where a supervisor creates a new virtual instruction that is essentially a jump instruction to jump to the newly-compiled native code. *See id.* at 296. The original virtual instruction is overwritten with the new jump instruction. *See id.* Execution of the new jump instruction directs execution of the newly-compiled native code. *See id.* at 291, 296.

Wakeling discloses generating a new virtual machine instruction that references native instructions, i.e., a new jump instruction that references the new native code (*see id.* at 288, 291, 296) and (a) executing the new virtual machine instruction instead of an original virtual machine instruction, i.e., executing the new jump instruction to direct execution of the new native code (*see id.* at 291, 296) and (b) executing the new virtual machine instruction after compiling of the function (*see id.* at 291 (describing "static and dynamic compilation of the program")). These

limitations, which are disclosed in this prior art reference, form the basis upon which the Patent Office determined the patentability of independent claims 1 and 8 of the '205 patent, respectively.

Wakeling also discloses the remaining limitations of independent claims 1 and 8 and dependent claims 2-4 of the '205 patent. Accordingly, a reasonable examiner would have considered the teachings of Wakeling to be important in determining whether or not the specified claims of the '205 patent were patentable. As set forth in detail in the Claim Chart in Exhibit 12, Wakeling anticipates claims 1-4 and 8 of the '205 patent. For this reason, Wakeling raises a substantial new question of patentability with respect to claims 1-4 and 8 of the '205 patent.

Lewis: Brian T. Lewis et al., *Clarity MCode: A Retargetable Intermediate Representation for Compilation*, ACM, IR '95, 1/95, San Francisco, California, USA, pp. 119-128, 1995 (hereinafter, "Lewis"), provided as Exhibit 4, is a publication directed to compiling of Clarity C++ programming language. Because Lewis was published in 1995, it is prior art under 35 U.S.C. § 102(b) to the '205 patent, given that the earliest possible priority date for the '205 patent is June 30, 1997. Lewis was not in front of the Patent Office during the prosecution of the application that matured into the '205 patent, and it is not cumulative to the prior art considered by the Patent Office during the prosecution of the '205 patent.

Lewis relates to "middle code" ("MCode") that compiles programs at execution time. *See* Lewis at 119. In operation, when a specified call threshold is reached, a machine code generator is run the next time the procedure is called. *See id.* at 126. This action is performed by rewriting the procedure's trampoline instructions to jump to the on-the-fly compiler instead of the MCode interpreter. *See id.* When the compiler is finished, it rewrites the trampoline to jump

to the generated machine code and then jumps to the code itself. *See id.* Thereafter, execution of the new trampoline instruction directs execution of the generated machine code. *See id.*

Lewis discloses generating a new virtual machine instruction that references native instructions, i.e., the new trampoline instruction that references the generated machine code (*see id.*) and (a) executing the new virtual machine instruction instead of an original virtual machine instruction, i.e., executing the new trampoline instruction to direct execution of the generated machine code (s*ee id.*) and (b) executing the new virtual machine instruction after compiling of the function (s*ee id.*; *see id.* at 119 (describing compilation of programs at run time)). These limitations, which are disclosed in this prior art reference, form the basis upon which the Patent Office determined the patentability of independent claims 1 and 8 of the '205 patent, respectively.

Lewis also discloses the remaining limitations of independent claims 1 and 8 and dependent claims 2-4 of the '205 patent. Accordingly, a reasonable examiner would have considered the teachings of Lewis to be important in determining whether or not the specified claims of the '205 patent were patentable. As set forth in detail in the Claim Chart in Exhibit 13, Lewis anticipates claims 1-4 and 8 of the '205 patent. For this reason, Lewis raises a substantial new question of patentability with respect to claims 1-4 and 8 of the '205 patent.

Tarau: Paul Tarau et al., *The Power of Partial Translation: An Experiment with the C-Ification of Binary Prolog*, ACM Symposium on Applied Computing, pp. 152-156, 1995 (hereinafter, "Tarau"), provided as Exhibit 5, is a publication directed to compiling portions of emulator instructions to native code, leaving virtual code and native code instructions. Because Tarau was published in 1995, it is prior art under 35 U.S.C. § 102(b) to the '205 patent, given that the earliest possible priority date for the '205 patent is June 30, 1997. Tarau was not in front

of the Patent Office during the prosecution of the application that matured into the '205 patent, and it is not cumulative to the prior art considered by the Patent Office during the prosecution of the '205 patent.

Tarau relates to a translation framework that compiles sequences of emulator instructions to native code. *See* Tarau at Abstract. After compiling virtual machine code to native code, byte code may be modified to represent or reference the native code to effect the transition between interpreting byte code and executing native code. *See id.* at 153. Then, the modified byte code is executed, which references the native code for execution. *See id.* at 155.

Tarau discloses generating a new virtual machine instruction that references native instructions, i.e., modifying the byte code to reference the machine code (s*ee id.* at 153) and (a) executing the new virtual machine instruction instead of an original virtual machine instruction, i.e., executing the modified byte code to direct execution of the machine code (s*ee id.* at 153, 155) and (b) executing the new virtual machine instruction after compiling of the function (s*ee id.* at 152 (describing compilation of the native and machine code together to a stand alone executable)). These limitations, which are disclosed in this prior art reference, form the basis upon which the Patent Office determined the patentability of independent claims 1 and 8 of the '205 patent, respectively.

Tarau also discloses the remaining limitations of independent claims 1 and 8 and dependent claims 2-4 of the '205 patent. Accordingly, a reasonable examiner would have considered the teachings of Tarau to be important in determining whether or not the specified claims of the '205 patent were patentable. As set forth in detail in the Claim Chart in Exhibit 14, Tarau anticipates claims 1-4 and 8 of the '205 patent. For this reason, Tarau raises a substantial new question of patentability with respect to claims 1-4 and 8 of the '205 patent.

Yellin: Frank Yellin, *The JIT Compiler API*, The JIT Compiler API, October 4, 1996, pp. 1-23 (hereinafter, "Yellin"), provided as Exhibit 6, is a publication directed to generating native code instructions for portions of programming running in a Java Virtual Machine. Because Yellin was published in October 1996, it is prior art under 35 U.S.C. § 102(a) to the '205 patent, given that the earliest possible priority date for the '205 patent is June 30, 1997. Yellin was not in front of the Patent Office during the prosecution of the application that matured into the '205 patent, and it is not cumulative to the prior art considered by the Patent Office during the prosecution of the '205 patent.

Yellin is directed to native code generators that run insde the Java Virtual Machine. *See* Yellin at 1. "Fat" class files comprising both Java byte code and corresponding native code are compiled. *See id.* The fat class file includes the original byte code definitions of all methods and alternative native machine code definitions for some of the methods. *See id.* In addition, Yellin discloses API tools for replacing byte code with new byte code that is used to execute the native code. *See id.* at 3-4. After compiling native code, the new byte code is used instead of pre-existing byte code to execute the native code. *See id.*

Yellin discloses generating a new virtual machine instruction that references native instructions, i.e., the new byte code that replaces the existing byte code and that references the native code (s*ee* Yellin at 3-4) and (a) executing the new virtual machine instruction instead of an original virtual machine instruction, i.e., executing the new byte code to direct execution of the native code (s*ee id.*) and (b) executing the new virtual machine instruction after compiling of the function (s*ee id.* at 1 (compiled programs include the virtual and machine instructions)). These limitations, which are disclosed in this prior art reference, form the basis upon which the

Patent Office determined the patentability of independent claims 1 and 8 of the '205 patent, respectively.

Yellin also discloses the remaining limitations of independent claims 1 and 8 and dependent claims 2-4 of the '205 patent. Accordingly, a reasonable examiner would have considered the teachings of Yellin to be important in determining whether or not the specified claims of the '205 patent were patentable. As set forth in detail in the Claim Chart in Exhibit 15, Yellin anticipates claims 1-4 and 8 of the '205 patent. For this reason, Yellin raises a substantial new question of patentability with respect to claims 1-4 and 8 of the '205 patent.

Nilsen '665 Patent: U.S. Patent No. 6,081,665 to Nilsen et al, entitled "Method for Efficient Soft Real-Time Execution of Portable Byte Code computer Programs," issued on June 27, 2000 from an application filed December 19, 1997, with priority to December 21, 1996 (hereinafter, the "Nilsen '665 patent"), provided as Exhibit 7. The Nilsen '665 patent is a U.S. patent directed to generating portions of virtual machine instructions into a new instruction set that more efficiently manipulates multiple stacks of virtual machine instructions. Because the Nilsen '665 patent is based on an application filed December 21, 1996, it is prior art under 35 U.S.C. § 102(e) to the '205 patent, given that the earliest possible priority date for the '205 patent is June 30, 1997. The Nilsen '665 patent was not in front of the Patent Office during the prosecution of the application that matured into the '205 patent, and it is not cumulative to the prior art considered by the Patent Office during the prosecution of the '205 patent.

The Nilsen '665 patent is particularly relevant given the patent owner's admissions in the Oracle v. Google litigation. The Nilsen '665 patent discloses pointers in a table to native code (*see* the Nilsen '665 patent at 13:48-14:14), which the patent owner considers are substantially the same as the claimed new virtual machine instruction (*see* Oracle America, Inc.'s Preliminary

Infringement Contentions for the '205 Patent at Exhibit B-1, pp. 42-43). Specifically, the Nilsen '665 patent discloses generating a new "PERC" virtual machine instruction, which replaces an original virtual machine instruction. S*ee id*; *see id.* at 63:64-65:41. The new PERC virtual machine instruction points to native machine instructions created by a just-in-time compiler. *See id.* at 13:48-14:14. Execution of the new PERC virtual machine instruction, instead of the original virtual machine instruction, directs execution of the native machine instructions. *See id.*

In light of the patent owner's admissions in the Oracle v. Google litigation, the Nilsen '665 patent discloses generating a new virtual machine instruction that references native instructions, i.e., the new PERC virtual machine instruction that points to native machine instructions (s*ee* the Nilsen '665 patent at 5:66-6:33; 12:37-49; 13:48-14:14; 63:64-65:41) and (a) executing the new virtual machine instruction instead of an original virtual machine instruction, i.e., execution of the new PERC virtual machine instruction, instead of the original virtual machine instruction, directs execution of the native machine instructions (*see id.* at 5:66-6:33; 13:48-14:14; 63:64-65:41) and (b) executing the new virtual machine instruction after compiling of the function (s*ee id.* at 63:64-65:41 (discussing integration of the compiled function)). These limitations, which are disclosed in this prior art reference, form the basis upon which the Patent Office determined the patentability of independent claims 1 and 8 of the '205 patent, respectively.

The Nilsen '665 patent also discloses the remaining limitations of independent claims 1 and 8 and dependent claims 2-4 of the '205 patent. Accordingly, a reasonable examiner would have considered the teachings of the Nilsen '665 patent to be important in determining whether or not the specified claims of the '205 patent were patentable. As set forth in detail in the Claim Chart in Exhibit 16, the Nilsen '665 patent anticipates claims 1-4 and 8 of the '205 patent. For

this reason, the Nilsen '665 patent raises a substantial new question of patentability with respect to claims 1-4 and 8 of the '205 patent.

Hookway '017 Patent: U.S. Patent No. 5,842,017 to Hookway et al., entitled "Method and Apparatus for Forming a Translation Unit," issued November 24, 1998 from an application filed January 29, 1996 (hereinafter, the "Hookway '017 patent"), provided as Exhibit 8. The Hookway '017 patent is a U.S. patent directed to a computer system that converts instructions from an instruction set of a first, non-native computer system to a second, different native computer system for execution at run-time. Because the Hookway '017 patent is based on an application filed January 29, 1996, it is prior art under 35 U.S.C. § 102(e) to the '205 patent, given that the earliest possible priority date for the '205 patent is June 30, 1997. The Hookway '017 patent was not in front of the Patent Office during the prosecution of the application that matured into the '205 patent, and it is not cumulative to the prior art considered by the Patent Office during the prosecution of the '205 patent.

The Hookway '017 patent is particularly relevant given the patent owner's admissions in the Oracle v. Google litigation. The Hookway '017 patent discloses pointers to native code (*see* the Hookway '017 patent at 10:16-21; 12:17-52), which the patent owner considers are substantially the same as the claimed new virtual machine instruction (*see* Oracle America, Inc.'s Preliminary Infringement Contentions for the '205 Patent at Exhibit B-1, pp. 42-43). Specifically, the Hookway '017 patent discloses generating addresses for identifying and executing native instructions instead of virtual machine instructions *See id.* The indicators (considered by the patent owner to be insubstantially different from the claimed new machine instructions) direct execution of the native instructions *See id.* at 9:31-48, 10:16-21; 12:17-52.

In light of the patent owner's admissions in the Oracle v. Google litigation, the Hookway '017 patent discloses generating a new virtual machine instruction that references native instructions, i.e., the new addresses that point to the native instructions (see *id.* at 3:47-53; 9:61-10:6; 10:16-21; 10:38-45; 11:64-12:16; 13:9-27; 13:45-57) and (a) executing the new virtual machine instruction instead of an original virtual machine instruction, i.e., executing the address to direct execution of the corresponding native instruction (see *id.* at 9:31-48; 10:16-21; 12:17-52; 13:4-8; 15:9-22) and (b) executing the new virtual machine instruction after compiling of the function (see *id.* at 9:31-48; 10:16-21; 12:17-52; 13:4-8; 13:45-57; 15:9-22 (execution of the function after creation of the new native instructions and mapping to the new native instructions within the virtual machine instructions). These limitations, which are disclosed in this prior art reference, form the basis upon which the Patent Office determined the patentability of independent claims 1 and 8 of the '205 patent, respectively.

The Hookway '017 patent also discloses the remaining limitations of independent claims 1 and 8 and dependent claims 2-4 of the '205 patent. Accordingly, a reasonable examiner would have considered the teachings of the Hookway '017 patent to be important in determining whether or not the specified claims of the '205 patent were patentable. As set forth in detail in the Claim Chart in Exhibit 17, the Hookway '017 patent anticipates claims 1-4 and 8 of the '205 patent. For this reason, the Hookway '017 patent raises a substantial new question of patentability with respect to claims 1-4 and 8 of the '205 patent.

Magnusson: Peter Magnusson, *Partial Translation*, Swedish Institute of Computer Science Technical Report (T93.5), Oct. 1993 (hereinafter, "Magnusson"), provided as Exhibit 9, is a publication directed to a combining block translation and interpretive translation in an intermediate format that supports the addition of run-time generated code. Because Magnusson

was published in 1993, it is prior art under 35 U.S.C. § 102(b) to the '205 patent, given that the earliest possible priority date for the '205 patent is June 30, 1997. Magnusson was not in front of the Patent Office during the prosecution of the application that matured into the '205 patent, and it is not cumulative to the prior art considered by the Patent Office during the prosecution of the '205 patent.

Magnusson relates to "partial translation" of native instructions by combining the benefits of traditional block translation and interpretive translation. A portion of virtual machine instructions is compiled into a native machine instruction, and a pointer or a "translated" instruction is inserted in the original virtual machine instructions. *See* Magnusson at 9. Executing the pointer or "translated" instruction directs execution of the native machine instruction. *See id.*

Magnusson discloses generating a new virtual machine instruction that references native instructions, i.e., the translated instruction that references the native instruction (s*ee* Magnusson at 8-9) and (a) executing the new virtual machine instruction instead of an original virtual machine instruction, i.e., executing the translated instruction to direct execution of the native instruction (s*ee id.* at 10-12) and (b) executing the new virtual machine instruction after compiling of the function (s*ee id.* at 9 (execution of the translated instruction after the virtual instructions are compiled). These limitations, which are disclosed in this prior art reference, form the basis upon which the Patent Office determined the patentability of independent claims 1 and 8 of the '205 patent, respectively.

Magnusson also discloses the remaining limitations of independent claims 1 and 8 and dependent claims 2-4 of the '205 patent. Accordingly, a reasonable examiner would have considered the teachings of Magnusson to be important in determining whether or not the

specified claims of the '205 patent were patentable. As set forth in detail in the Claim Chart in Exhibit 18, Magnusson anticipates claims 1-4 and 8 of the '205 patent. For this reason, Magnusson raises a substantial new question of patentability with respect to claims 1-4 and 8 of the '205 patent.

The Walters '593 Patent: U.S. Patent No. 5,768,593 to Walters et al., entitled "Dynamic Cross-Compilation System and Method," issued June 16, 1998 from an application filed March 22, 1996 (hereinafter, the "Walters '593 patent"), provided as Exhibit 10. The Walters '593 patent is a U.S. patent directed to a computer system that converts non-native code into native code immediately prior to execution of that code. Because the Walters '593 patent is based on an application filed March 22, 1996, it is prior art under 35 U.S.C. § 102(e) to the '205 patent, given that the earliest possible priority date for the '205 patent is June 30, 1997.

The Walters '593 patent was the main reference considered by the Patent Office during the prosecution of the application that matured into the '205 patent. Nevertheless, substantial new questions of patentability based on the Walters '593 patent still exist. See 35 U.S.C. § 312(a) ("The existence of a substantial new question of patentability is not precluded by the fact that a patent or printed publication was previously cited by or to the Office or considered by the Office."). During prosecution of the '205 patent, the Patent Office indicated that independent claims 1 and 8 were patentable over the Walters '593 patent because the Walters '593 patent allegedly failed to teach executing the new virtual instruction instead of the original virtual instruction (claim 1) and executing the new virtual instruction after the compiling of the function (claim 8). *See* Notice of Allowance dated January 13, 2005, at p. 2. However, as discussed previously, each of Deutsch, Wakeling, Lewis, Tarau, Yellin, the Nilsen '665 patent, the Hookway '017 patent, and Magnusson (collectively, the "non-considered prior art") disclose

these limitations recited in claims 1 and 8 of the '205 patent. Additionally, a person having ordinary skill in the art at the time of the invention of the '205 patent would have found it obvious to include the teachings of the non-considered prior art with the teachings of the Walters '593 patent to create methods recited in claims 1-4 and 8 of the '205 patent.

Accordingly, a reasonable examiner would have considered the teachings of the Walters '593 patent combined with the teachings of the non-considered prior art to be important in determining whether or not the specified claims of the '205 patent were patentable. As set forth in detail in the Claim Chart in Exhibit 19, claims 1-4 and 8 of the '205 patent are obvious over the Walters '593 patent in view of each of the non-considered prior art. For these reasons, the Walters '593 patent raises substantial new questions of patentability with respect to claims 1-4 and 8 of the '205 patent.

III. DETAILED EXPLANATION UNDER 37 C.F.R. § 1.915(B)(3) OF THE PERTINENCY AND MANNER OF APPLYING THE CITED PRIOR ART TO EVERY CLAIM FOR WHICH REEXAMINATION IS REQUESTED

The detailed explanation herein under 37 C.F.R. § 1.915(b)(3) is set forth in the attached detailed Claim Charts. This detailed explanation describes the pertinence and manner of applying the prior art references to the claims of the '205 patent.

A. Anticipation Under 35 U.S.C. § 102

1. Claims 1-4 and 8 are unpatentable under 35 U.S.C. § 102(b) as being anticipated by Deutsch.

As discussed above, Deutsch is prior art to the '205 patent. And, as set forth in detail in the Claim Chart attached as Exhibit 11, Deutsch anticipates each of claims 1-4 and 8 of the '205 patent.

2. Claims 1-4 and 8 are unpatentable under 35 U.S.C. § 102(b) as being anticipated by Wakeling.

As discussed above, Wakeling is prior art to the '205 patent. And, as set forth in detail in the Claim Chart attached as Exhibit 12, Wakeling anticipates each of claims 1-4 and 8 of the '205 patent.

3. Claims 1-4 and 8 are unpatentable under 35 U.S.C. § 102(b) as being anticipated by Lewis.

As discussed above, Lewis is prior art to the '205 patent. And, as set forth in detail in the Claim Chart attached as Exhibit 13, Lewis anticipates each of claims 1-4 and 8 of the '205 patent.

4. Claims 1-4 and 8 are unpatentable under 35 U.S.C. § 102(b) as being anticipated by Tarau.

As discussed above, Tarau is prior art to the '205 patent. And, as set forth in detail in the Claim Chart attached as Exhibit 14, Tarau anticipates each of claims 1-4 and 8 of the '205 patent.

5. Claims 1-4 and 8 are unpatentable under 35 U.S.C. § 102(a) as being anticipated by Yellin.

As discussed above, Yellin is prior art to the '205 patent. And, as set forth in detail in the Claim Chart attached as Exhibit 15, Yellin anticipates each of claims 1-4 and 8 of the '205 patent.

6. Claims 1-4 and 8 are unpatentable under 35 U.S.C. § 102(e) as being anticipated by the Nilsen '665 patent.

As discussed above, the Nilsen '665 patent is prior art to the '205 patent. And, as set forth in detail in the Claim Chart attached as Exhibit 16, the Nilsen '665 patent anticipates each of claims 1-4 and 8 of the '205 patent.

7. Claims 1-4 and 8 are unpatentable under 35 U.S.C. § 102(e) as being anticipated by the Hookway '017 patent.

As discussed above, the Hookway '017 patent is prior art to the '205 patent. And, as set forth in detail in the Claim Chart attached as Exhibit 17, the Hookway '017 patent anticipates each of claims 1-4 and 8 of the '205 patent.

8. Claims 1-4 and 8 are unpatentable under 35 U.S.C. § 102(b) as being anticipated by Magnusson.

As discussed above, Magnusson is prior art to the '205 patent. And, as set forth in detail in the Claim Chart attached as Exhibit 18, Magnusson anticipates each of claims 1-4 and 8 of the '205 patent.

B. Obviousness Under 35 U.S.C. § 103(a)

1. Claims 1-4 and 8 are unpatentable under 35 U.S.C. § 103(a) as being obvious over the Walters '593 patent in view of Deutsch.

As discussed above, the Walters '593 patent and Deutsch are prior art to the '205 patent. And, as set forth in detail in the Claim Chart attached as Exhibit 19, the Walters '593 patent in view of Deutsch renders obvious each of claims 1-4 and 8 of the '205 patent.

2. Claims 1-4 and 8 are unpatentable under 35 U.S.C. § 103(a) as being obvious over the Walters '593 patent in view of Wakeling.

As discussed above, the Walters '593 patent and Wakeling are prior art to the '205 patent. And, as set forth in detail in the Claim Chart attached as Exhibit 19, the Walters '593 patent in view of Wakeling renders obvious each of claims 1-4 and 8 of the '205 patent.

3. Claims 1-4 and 8 are unpatentable under 35 U.S.C. § 103(a) as being obvious over the Walters '593 patent in view of Lewis.

As discussed above, the Walters '593 patent and Lewis are prior art to the '205 patent. And, as set forth in detail in the Claim Chart attached as Exhibit 19, the Walters '593 patent in view of Lewis renders obvious each of claims 1-4 and 8 of the '205 patent.

4. Claims 1-4 and 8 are unpatentable under 35 U.S.C. § 103(a) as being obvious over the Walters '593 patent in view of Tarau.

As discussed above, the Walters '593 patent and Tarau are prior art to the '205 patent. And, as set forth in detail in the Claim Chart attached as Exhibit 19, the Walters '593 patent in view of Tarau renders obvious each of claims 1-4 and 8 of the '205 patent.

5. Claims 1-4 and 8 are unpatentable under 35 U.S.C. § 103(a) as being obvious over the Walters '593 patent in view of Yellin.

As discussed above, the Walters '593 patent and Yellin are prior art to the '205 patent. And, as set forth in detail in the Claim Chart attached as Exhibit 19, the Walters '593 patent in view of Yellin renders obvious each of claims 1-4 and 8 of the '205 patent.

6. Claims 1-4 and 8 are unpatentable under 35 U.S.C. § 103(a) as being obvious over the Walters '593 patent in view of the Nilsen '665 patent.

As discussed above, the Walters '593 patent and the Nilsen '665 patent are prior art to the '205 patent. And, as set forth in detail in the Claim Chart attached as Exhibit 19, the Walters '593 patent in view of the Nilsen '665 patent renders obvious each of claims 1-4 and 8 of the '205 patent.

7. Claims 1-4 and 8 are unpatentable under 35 U.S.C. § 103(a) as being obvious over the Walters '593 patent in view of the Hookway '017.

As discussed above, the Walters '593 patent and the Hookway '017 are prior art to the '205 patent. And, as set forth in detail in the Claim Chart attached as Exhibit 19, the Walters '593 patent in view of the Hookway '017 renders obvious each of claims 1-4 and 8 of the '205 patent.

8. Claims 1-4 and 8 are unpatentable under 35 U.S.C. § 103(a) as being obvious over the Walters '593 patent in view of Magnusson.

As discussed above, the Walters '593 patent and Magnusson are prior art to the '205 patent. And, as set forth in detail in the Claim Chart attached as Exhibit 19, the Walters '593 patent in view of Magnusson renders obvious each of claims 1-4 and 8 of the '205 patent.

IV. CONCLUSION

For the reasons provided herein, Requester respectfully submits that the prior art submitted herewith raises substantial new questions of patentability as to claims 1-4 and 8 of the '205 patent because, as discussed above, claims 1-4 and 8 of the '205 patent are anticipated by and/or rendered obvious in view of the prior art patents and printed publications discussed herein. Accordingly, reexamination of claims 1-4 and 8 of the '205 patent is respectfully requested, finally rejecting these claims.

The undersigned further notes the standards set forth at 37 C.F.R. § 1.903 wherein the reexamination Requesters will be sent copies of Office Actions issued during the reexamination proceedings as well as served (by the patent owner) with any document filed in the reexamination proceeding in accordance with 37 C.F.R. 1.248. *See* MPEP §§ 2664 and 2666.

If the Patent Office determines that a fee and/or other relief is required, Requester petitions for any required relief including authorizing the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to **Deposit Account No. 11-0980** referencing Docket No. 13557.112021.

As identified in the attached Certificate of Service and in accordance with 37 C.F.R. §§ 1.33(c) and 1.915(b)(6), a copy of the present request is being served to the address of the attorney or agent of record for the '205 patent.

February 17, 2011

Respectfully submitted,

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