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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.



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CENTRAL REEXAMINATION UNIT

**Transmittal of Communication to Third Party Requester
Inter Partes Reexamination**

REEXAMINATION CONTROL NO. : 95001548
PATENT NO. : 6910205
TECHNOLOGY CENTER : 3999
ART UNIT : 3992

Enclosed is a copy of the latest communication from the United States Patent and Trademark Office in the above identified Reexamination proceeding. 37 CFR 1.903.

Prior to the filing of a Notice of Appeal, each time the patent owner responds to this communication, the third party requester of the inter partes reexamination may once file written comments within a period of 30 days from the date of service of the patent owner's response. This 30-day time period is statutory (35 U.S.C. 314(b)(2)), and, as such, it cannot be extended. See also 37 CFR 1.947.

If an ex parte reexamination has been merged with the inter partes reexamination, no responsive submission by any ex parte third party requester is permitted.

All correspondence relating to this inter partes reexamination proceeding should be directed to the Central Reexamination Unit at the mail, FAX, or hand-carry addresses given at the end of the communication enclosed with this transmittal.

Transmittal of Communication to Third Party Requester Inter Partes Reexamination	Control No.	Patent Under Reexamination	
	95/001,548	6910205	
	Examiner	Art Unit	
	ERIC B. KISS	3992	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address. --

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Prior to the filing of a Notice of Appeal, each time the patent owner responds to this communication, the third party requester of the *inter partes* reexamination may once file written comments within a period of 30 days from the date of service of the patent owner's response. This 30-day time period is statutory (35 U.S.C. 314(b)(2)), and, as such, it cannot be extended. See also 37 CFR 1.947.

If an *ex parte* reexamination has been merged with the *inter partes* reexamination, no responsive submission by any *ex parte* third party requester is permitted.

All correspondence relating to this inter partes reexamination proceeding should be directed to the **Central Reexamination Unit** at the mail, FAX, or hand-carry addresses given at the end of the communication enclosed with this transmittal.

ORDER GRANTING/DENYING REQUEST FOR INTER PARTES REEXAMINATION	Control No.	Patent Under Reexamination	
	95/001,548	6910205	
	Examiner	Art Unit	
	ERIC B. KISS	3992	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address. --

The request for *inter partes* reexamination has been considered. Identification of the claims, the references relied on, and the rationale supporting the determination are attached.

Attachment(s): ☐ PTO-892 ☒ PTO/SB/08 ☐ Other: _____

1. ☒ The request for *inter partes* reexamination is GRANTED.

☐ An Office action is attached with this order.

☒ An Office action will follow in due course.

2. ☐ The request for *inter partes* reexamination is DENIED.

This decision is not appealable. 35 U.S.C. 312(c). Requester may seek review of a denial by petition to the Director of the USPTO within ONE MONTH from the mailing date hereof. 37 CFR 1.927. EXTENSIONS OF TIME ONLY UNDER 37 CFR 1.183. In due course, a refund under 37 CFR 1.26(c) will be made to requester.

All correspondence relating to this *inter partes* reexamination proceeding should be directed to the **Central Reexamination Unit** at the mail, FAX, or hand-carry addresses given at the end of this Order.

ORDER GRANTING *INTER PARTES* REEXAMINATION

A substantial new question of patentability affecting claims 1-4 and 8 of United States Patent 6,910,205 is raised by the present request for *inter partes* reexamination.

Extensions of time under 37 CFR 1.136(a) will not be permitted in *inter partes* reexamination proceedings because the provisions of 37 CFR 1.136 apply only to “an applicant” and not to the patent owner in a reexamination proceeding. Additionally, 35 U.S.C. 314(c) requires that *inter partes* reexamination proceedings “will be conducted with special dispatch” (37 CFR 1.937). Patent owner extensions of time in *inter partes* reexamination proceedings are provided for in 37 CFR 1.956. Extensions of time are not available for third party requester comments, because a comment period of 30 days from service of patent owner’s response is set by statute. 35 U.S.C. 314(b)(3).

The patent owner is reminded of the continuing responsibility under 37 CFR 1.985(a), to apprise the Office of any litigation activity, or other prior or concurrent proceeding, involving Patent 6,910,205 throughout the course of this reexamination proceeding. The third party requester is also reminded of the ability to similarly apprise the Office of any such activity or proceeding throughout the course of this reexamination proceeding. See MPEP § 2686 and 2686.04.

I. IDENTIFICATION OF EVERY CLAIM FOR WHICH REEXAMINATION IS REQUESTED

Reexamination of claims 1-4 and 8 of the '205 patent has been requested. (Request for *Inter Partes* Reexamination, 2/17/2011, p. 1.)

II. REFERENCES CITED IN THE REQUEST

The request cites the following patents and printed publications as raising a substantial new question of patentability:

1. L. Peter Deutsch et al., *Efficient Implementation of the Smalltalk-80 System*, Proceedings of the 11th ACM SIGACT-SIGPLAN Symposium on Principles of Programming Languages, pp. 297-302, 1984 (hereinafter, "Deutsch");
2. David Wakeling, *A Throw-Away Compiler for a Lazy Functional Language*, Fuji International Workshop on Functional and Logic Programming, pp. 287-300, 1995 (hereinafter, "Wakeling");
3. Brian T. Lewis et al., *Clarity MCode: A Retargetable Intermediate Representation for Compilation*, ACM, IR '95, 1/95, San Francisco, California, USA, pp. 119-128, 1995 (hereinafter, "Lewis");
4. Paul Tarau et al., *The Power of Partial Translation: An Experiment with the Compilation of Binary Prolog*, ACM Symposium on Applied Computing, pp. 152-156, 1995 (hereinafter, "Tarau");
5. Frank Yellin, *The JIT Compiler API*, The JIT Compiler API, October 4, 1996, pp. 1-23 (hereinafter, "Yellin");
6. U.S. Patent 6,081,665 (Nilsen et al.);

7. U.S. Patent 5,842,017 (Hookway et al.);
8. Peter Magnusson, *Partial Translation*, Swedish Institute of Computer Science Technical Report (T93.5), Oct. 1993 (hereinafter, "Magnusson"); and
9. U.S. Patent 5,768,593 (Walters et al.).

III. PROSECUTION HISTORY

The '205 patent issued from application 10/194,040, filed July 12, 2002, as a continuation of application 08/884,856, now patent 6,513,156. Claims 1-4 and 8 of the '205 patent correspond to the '040 application's claims 32, 2-4, and 33, respectively.

In the first Office action on the merits in the '040 application (addressing original claims 1-31), the examiner rejected several claims under 35 U.S.C. § 102(e) as being anticipated by the Walters '593 patent. '040 App., Non-Final Rejection, 3/5/2004.

In response, the applicants added new claims 32 and 33 (and amended claim 2 to depend from claim 32), asserting that Walters did not teach or suggest "generating, at runtime, a new virtual machine instruction that represents or references one or more native instructions that can be executed instead of a first virtual machine instruction," as found in claim 32, or "representing at least one native machine instruction with a virtual machine instruction that is executed after compiling the function," as found in claim 33. '040 App., Remarks 6/1/2004, p. 12.

The examiner disagreed with the applicants' arguments, finding that the Walters '593 patent disclosure of cross-compiling an application such that some parts are native code and some are native code blocks met the language of claim 33, including representing that at least one native machine instruction with a virtual machine instruction (non-native instruction) that is executed after the compiling of the function. '040 App., Final Rejection, 9/23/2004. All of the

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pending claims were rejected under the doctrine of nonstatutory double patenting as being unpatentable over claims 1-47 of U.S. Pat. 6,513,156 (issued from the parent application), and claims 1, 8-12, 21, 22, 29-31, 33-36, and 38-41 were rejected under § 102(e) as being anticipated by the Walters '593 patent, but claims 2-7, 32, and 37 were not rejected on the basis of prior art¹.

Id.

The applicants canceled claims 1, 8-12, 21, 22, and 29-31, leaving claims 2-7 and 32-41 the only remaining pending claims. A terminal disclaimer was filed to overcome the double patenting rejection. '404 App., Amendment, 10/7/2004.

In an Advisory Action, the examiner allowed claims 2-7 and 32 but maintained the rejection of claims 33-41 under § 102(e). The examiner compared the limitations in allowable claim 32 with those in rejected claim 33:

Claim 32 details generating a new virtual machine instruction that is executed instead of a first virtual machine instruction and represents one or more native instructions wherein the new virtual machine instruction is executed instead of the first virtual machine instructions. Claim 33 does not read upon this same interpretation. Claim 33 details inputting virtual machine instructions, compiling a portion of the instructions wherein at least one native machine instruction is represented by a virtual machine instruction. In claim 33, the represented virtual [machine] instruction is the same virtual [machine] instruction inputted. Therefore, one simply compiles a portion of the overall function and executes the whole function by determining if the next virtual [machine] instruction of the function is precompiled or not and acting accordingly by directly executing the native code or interpreting and executing the instruction. The cited prior art of record allows for this and therefore the rejection is maintained.

'404 App., Advisory Action, 12/14/2004.

On January 3, 2005, an interview was conducted during which the applicants' representative proposed to amend claim 33 wherein the native machine instruction is represented

¹ The Final Rejection stated on p. 3 that claims 1, 8-12, 19-22, and 29-31 were rejected under § 102(e), but in the discussion of the rejection, the limitations of claims 1, 8-12, 21, 22, 29-31, 33-36, and 38-41 were mapped to the teachings of the Walters '593 patent.

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with a new virtual machine instruction that is executed after the compiling of the function. The examiner agreed and entered an Examiner's Amendment, inserting the word "new" into the final limitation of claim 33, changing it to its patented language, "representing said at least one native machine instruction with a new virtual machine instruction that is executed after the compiling of the function." '040 App., Examiner's Amendment, 1/13/2005 (underlining in original to indicate amended matter). The examiner provided detailed reasons for allowance:

Claims 32 and 2-7 teach generating at run-time a new virtual machine instruction that represents one or more native instructions that can be executed instead of a first virtual machine instruction.

Claim 33 teaches compiling a portion of virtual machine instructions into at least one native machine instruction wherein the native machine instruction is represented with a new virtual machine instruction that is executed after the compiling of the function.

Claims 34, 35, and 38-41 teaches a hybrid virtual and native machine instruction data structure which stores a copy of a selected virtual machine instruction that was overwritten in the sequence of virtual machine instructions by the new virtual machine instruction.

The cited prior art of record, in particular Walters, teaches a technique for increasing the speed of executing non-native applications, i.e. bytecodes, by cross-compiling portions of the application that would be beneficial in native code for faster execution into native instructions and having the entry bytecode for the compiled instructions point to location of the stored native instructions. Therefore, when the application is executed, a determination is made to see if the current bytecode is an entry bytecode. If this determination is positive, the corresponding set of native instruction(s) is executed. If this determination is negative, then the bytecode is interpreted and executed. The cited prior art of record however, does not teach or allude to the generation of a new virtual [machine] instruction that represents the one or more native instructions such that this new instruction is executed either (1) instead of the original virtual [machine] instruction or (2) after the compiling of the function. Walters makes the original non-native instruction an entry instruction for the native instructions, therefore, the original non-native instruction is always executed and no new virtual [machine] instruction is created to be executed. The cited prior art of record also does not teach or allude to the hybrid virtual-native instruction set maintaining a copy of the selected virtual [machine] instruction that was overwritten by the new virtual machine instruction. As stated above, Walters makes the original non-native instruction an entry instruction for the native instruction(s), therefore, the original non-native instruction is always executed and no new virtual [machine] instruction is created to be executed, yet alone overwrites an

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original virtual [machine] instruction such that both are stored in the overall hybrid virtual-native instruction set. Therefore, the claims are allowable over the cited prior art of record for at least the reasoning disclosed above.

'040 App., Notice of Allowability, 1/13/2005, pp. 2-4.

IV. SUBSTANTIAL NEW QUESTIONS OF PATENTABILITY (SNQ)

A. Deutsch

The request sets forth that the third party requester considers an SNQ as to claims 1-4 and 8 is raised by *Deutsch*, considered alone or in combination with the Walters '593 patent.

(Request at 23-25.) The examiner disagrees.

The request asserts that *Deutsch* teaches generating a new virtual machine instruction that references native instructions, i.e., creating a new call instruction from a virtual machine instruction which includes a translated procedure in native code and (a) executing the new virtual machine instruction instead of an original virtual machine instruction, i.e., executing the new call instruction and (b) executing the new virtual machine instruction after compiling of the function. (Request at 24 (citing *Deutsch* at 298-300).)

The cited portions of *Deutsch* appear to be concerned with translation of v-code (code in the instruction set of the Smalltalk-80 v-machine) into n-code (code that executes directly on the hardware without interpretation). *Deutsch* at 298, col. 1. In this way, *Deutsch* avoids interpretation overhead and gains the opportunity for certain types of optimizations. *Id.* at 298, col. 2. *Deutsch* further describes a dynamic translator that finds a v-code routine corresponding to a procedure about to be executed, translates it into n-code, and completes the call. *Id.* *Deutsch* addresses compatibility issues by generating special n-code that calls a subroutine to ensure that an object is represented in a form where accesses to its named parts are meaningful,

i.e. the runtime state is stored in a data structure (data object for procedure activation records) compatible with the v-machine. *Id.* at 299. For the actual execution of methods, Deutsch describes the generation of n-code calls that initially invoke a method-lookup to find the corresponding n-code method address and subsequently overwrite the n-code call with a call to the found address. *Id.* at 300.

Although the request asserts that Deutsch discloses generating a new virtual machine instruction (v-code instruction, using *Deutsch's* terminology), this does not appear to be the case. Because the disclosure of *Deutsch* does not appear to support the alleged new technological teaching set forth in the request, the request has not shown that there is a substantial likelihood that a reasonable examiner would consider *Deutsch* important in deciding whether or not claims 1-4 and 8 of the '205 patent are patentable. In the proposed combination of *Deutsch* and the Walters '593 patent, the requester asserts the same alleged new teaching in *Deutsch* as the basis for the proposed SNQ. Accordingly, *Deutsch*, considered alone or in combination with the Walters '593 patent, does not raise an SNQ as to claims 1-4 and 8.

B. Wakeling

The request sets forth that the third party requester considers an SNQ as to claims 1-4 and 8 is raised by *Wakeling*, considered alone or in combination with the Walters '593 patent. (Request at 25-26.) The examiner disagrees.

The request cites 3 different portions of *Wakeling* (p. 288 (describing prior approaches to interpreting code), p. 291 (describing the throw-away compilation technique that is used to execute X-code (a form of bytecode)), and p. 296 (describing an "idea that never made it" in which the cost of function calls was reduced by using self-modifying machine code). It appears that the requester relies on the teaching on p. 296 of *Wakeling* for the teaching of generating a

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new virtual machine instruction. (Request at 25.) Upon closer review, the cited portion of *Wakeling* appears to teach the same dynamic code modification technique taught by *Deutsch* as discussed above, where a native code instruction is overwritten once the address of compiled code is known. *Wakeling* at 296. This is described as the “don’t test, just enter” approach. *Id.* *Wakeling* describes the initial state of the dynamically-modifiable instruction as a jump to the supervisor, and after native code had been generated it was overwritten with a jump to that code. *Id.* This approach was abandoned by the author due to the overhead associated with cache coherency operations, system calls needed to flush any copies of the original native instruction already loaded into the instruction cache so that the replaced instruction would have to be loaded instead prior to execution. *Id.*; see also *id.* at 292 (further describing the cache coherency problems associated with throw-away compilation). There is no apparent teaching of a new virtual machine instruction being generated.

Because the disclosure of *Wakeling* does not appear to support the alleged new technological teaching set forth in the request, the request has not shown that there is a substantial likelihood that a reasonable examiner would consider *Wakeling* important in deciding whether or not claims 1-4 and 8 of the '205 patent are patentable. In the proposed combination of *Wakeling* and the Walters '593 patent, the requester asserts the same alleged new teaching in *Wakeling* as the basis for the proposed SNQ. Accordingly, *Wakeling*, considered alone or in combination with the Walters '593 patent, does not raise an SNQ as to claims 1-4 and 8.

C. Lewis

The request sets forth that the third party requester considers an SNQ as to claims 1-4 and 8 is raised by *Lewis*, considered alone or in combination with the Walters '593 patent. (Request at 26-27.) The examiner disagrees.

The request asserts that *Lewis* teaches generating a new virtual machine instruction that references native instructions, i.e., creating a new call instruction from a virtual machine instruction which includes a translated procedure in native code and (a) executing the new virtual machine instruction instead of an original virtual machine instruction, i.e., executing the new call instruction and (b) executing the new virtual machine instruction after compiling of the function. (Request at 26-27 (citing *Lewis* at 119 and 126).) The request specifically asserts that the rewritten trampoline instruction taught by *Lewis* is a new virtual machine instruction. However, the trampoline instructions taught by *Lewis* consist of platform-specific machine code rather than virtual machine code (consistent with the teachings of *Deutsch* and *Wakeling* discussed above). *Lewis* at 126, first paragraph.

Because the disclosure of *Lewis* does not appear to support the alleged new technological teaching set forth in the request, the request has not shown that there is a substantial likelihood that a reasonable examiner would consider *Lewis* important in deciding whether or not claims 1-4 and 8 of the '205 patent are patentable. In the proposed combination of *Lewis* and the Walters '593 patent, the requester asserts the same alleged new teaching in *Lewis* as the basis for the proposed SNQ. Accordingly, *Lewis*, considered alone or in combination with the Walters '593 patent, does not raise an SNQ as to claims 1-4 and 8.

D. Tarau

The request sets forth that the third party requester considers an SNQ as to claims 1-4 and 8 is raised by *Tarau*, considered alone or in combination with the Walters '593 patent. (Request at 27-28.) The examiner agrees.

As noted in the request, *Tarau* teaches modifying byte code to reference machine code and (a) executing the new virtual machine instruction instead of an original virtual machine instruction, i.e., executing the modified byte code to direct execution of the machine code and (b) executing the new virtual machine instruction after compiling of the function. (Request at 28 (citing *Tarau* at 152, 153, and 155).) Because this new, noncumulative technological teaching is relevant to the features asserted to be missing in the prior art in the examiner's reasons for allowance, there is a substantial likelihood that a reasonable examiner would consider *Tarau* important in deciding whether or not claims 1-4 and 8 of the '205 patent are patentable. Accordingly, *Tarau*, considered alone or in combination with the Walters '593 patent, raises an SNQ as to claims 1-4 and 8.

E. Yellin

The request sets forth that the third party requester considers an SNQ as to claims 1-4 and 8 is raised by *Yellin*, considered alone or in combination with the Walters '593 patent. (Request at 29-30.) The examiner disagrees.

The request cites pp. 3-4 of *Yellin* as allegedly teaching generating a new virtual machine instruction that references native instructions, i.e., the new byte code that replaces the existing byte code and that references the native code. (Request at 29 (citing *Yellin* at 3-4).) However, the cited portion of *Yellin* is directed to the use of quick codes, which utilize an unassigned bytecode to shadow another bytecode. A "quick" bytecode is a more efficient implementation of

the bytecode it replaces, but it still refers to byte code rather than referencing native code. In the example given on p. 4 of *Yellin*, a *string.length()* function, compiled into bytecode *invokevirtual #4*, is rewritten as bytecode *invokevirtual_quick 3 1* in order to avoid the overhead of checking whether the *String* class does in fact have a *length()* method, whether the current method is entitled to call the *length()* method, the location of the *length()* method within the *String* class's method table, and the total argument length of the *length()* method. Although a new virtual machine instruction is generated, the new instruction does not represent or reference native instructions.

Because the disclosure of *Yellin* does not appear to support the alleged new technological teaching set forth in the request, the request has not shown that there is a substantial likelihood that a reasonable examiner would consider *Yellin* important in deciding whether or not claims 1-4 and 8 of the '205 patent are patentable. In the proposed combination of *Yellin* and the Walters '593 patent, the requester asserts the same alleged new teaching in *Yellin* as the basis for the proposed SNQ. Accordingly, *Yellin*, considered alone or in combination with the Walters '593 patent, does not raise an SNQ as to claims 1-4 and 8.

F. The Nilsen '665 patent

The request sets forth that the third party requester considers an SNQ as to claims 1-4 and 8 is raised by the Nilsen '665 patent, considered alone or in combination with the Walters '593 patent. (Request at 30-32.) The examiner disagrees.

The request is extremely vague as to what specific portion in the Nilsen '665 patent corresponds to the new virtual machine instruction asserted to be taught, (see Request at 31 (citing portions of 8 different columns of *Nilsen* as allegedly teaching generating a new virtual

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machine instruction that references native instructions). However, it appears that the requester is equating a pointer table with the new virtual machine instruction.

The request relies in part on a pleading in the concurrent litigation, in which Oracle America, Inc. (the patent owner of record) argues that Google, Inc. (the real party in interest identified in the request for *inter partes* reexamination) is liable for infringing the '205 patent under the doctrine of equivalents. (Request at 20, 30-33.) The request highlights a portion of the infringement contention, reading "The differences, if any, between a 'new virtual machine instruction' and an entry in the jitEntry table are insubstantial," and asks the Office to accept the highlighted portion as a patent owner admission for the truth of the matter asserted². (*Id.* at 20.) The request attempts to further supplement or define the alleged admission by generalizing it to any pointer in a table to native code. (*Id.*) However, because the highlighted sentence, standing on its own, is not an admission relating to any prior art, and it is directed to matters affecting liability rather than patentability, it has no probative value in determining whether a substantial new question of patentability exists. *See* MPEP § 2617. The cited statements are given no weight as an admission appropriate for consideration during reexamination.

Because the request relies on improper evidence and vague assertions to support the alleged SNQ, the request fails to persuasively show that there is a substantial likelihood that a reasonable examiner would consider the Nilsen '665 patent important in deciding whether or not claims 1-4 and 8 of the '205 patent are patentable. In the proposed combination of the Nilsen '665 patent and the Walters '593 patent, the requester asserts the same alleged new teaching in the Nilsen '665 patent as the basis for the proposed SNQ. Accordingly, the Nilsen '665 patent,

² Presumably, the requester is *denying* this contention in the ongoing litigation rather than holding up any part of it as truth. The Office lacks the resources and jurisdiction to decide the issue either way.

considered alone or in combination with the Walters '593 patent, does not raise an SNQ as to claims 1-4 and 8.

G. The Hookway '017 patent

The request sets forth that the third party requester considers an SNQ as to claims 1-4 and 8 is raised by the Hookway '017 patent, considered alone or in combination with the Walters '593 patent. (Request at 32-33.) The examiner disagrees.

Similar to the proposed SNQ based on the Nilsen '665 patent, the request improperly relies on statements by the patent owner to support an assertion that a pointer table equates to the claimed generation of a virtual machine instruction. See the discussion of the Nilsen '665 patent above.

Because the disclosure of the Hookway '017 patent does not appear to support the alleged new technological teaching set forth in the request, the request has not shown that there is a substantial likelihood that a reasonable examiner would consider the Hookway '017 patent important in deciding whether or not claims 1-4 and 8 of the '205 patent are patentable. In the proposed combination of the Hookway '017 patent and the Walters '593 patent, the requester asserts the same alleged new teaching in the Hookway '017 patent as the basis for the proposed SNQ. Accordingly, the Hookway '017 patent, considered alone or in combination with the Walters '593 patent, does not raise an SNQ as to claims 1-4 and 8.

H. Magnusson

The request sets forth that the third party requester considers an SNQ as to claims 1-4 and 8 is raised by *Magnusson*, considered alone or in combination with the Walters '593 patent. (Request at 33-35.) The examiner agrees.

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As noted in the request, *Magnusson* teaches modifying virtual machine code (intermediate form code for a target machine simulator) to reference machine code and (a) executing the new virtual machine instruction (a “TRANSLATED” instruction) instead of an original virtual machine instruction, i.e., executing the modified virtual machine instruction to direct execution of the machine code and (b) executing the new virtual machine instruction after compiling of the function. (Request at 34 (citing *Magnusson* at 9).) Because this new, noncumulative technological teaching is relevant to the features asserted to be missing in the prior art in the examiner’s reasons for allowance, there is a substantial likelihood that a reasonable examiner would consider *Magnusson* important in deciding whether or not claims 1-4 and 8 of the ’205 patent are patentable. Accordingly, *Magnusson*, considered alone or in combination with the Walters ’593 patent, raises an SNQ as to claims 1-4 and 8.

VI. CONCLUSION

Claims 1-4 and 8 of U.S. Pat. 6,910,205 will be reexamined.

All correspondence relating to this *inter partes* reexamination proceeding should be directed:

By Mail to: Mail Stop *Inter Partes* Reexam
Attn: Central Reexamination Unit
Commissioner of Patents
United States Patent & Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

By FAX to: (571) 273-9900
Central Reexamination Unit

By hand: Customer Service Window
Randolph Building
401 Dulany St.
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Any inquiry concerning this communication or earlier communications from the examiner, or as to the status of this proceeding, should be directed to the Central Reexamination Unit at telephone number (571) 272-7705.

/Eric B. Kiss/
Primary Examiner, Art Unit 3992

Conferees:

A handwritten signature in black ink, appearing to be 'Eric B. Kiss', with a long horizontal flourish extending to the right.